Truesemi®

TSP50N20M

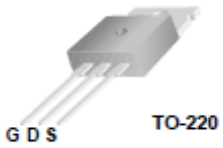
200V N-Channel MOSFET

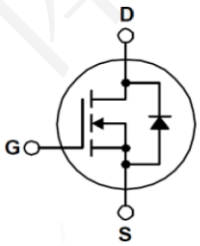
General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 50A,200V,Max.RDS(on)=0.051Ω @ VGS =10V
- Low gate charge: Qg=80nC (Typ.)
- Low drain-source On resistance: RDS(on)=51mΩ (Max.)
- 100% avalanche tested
- RoHS compliant device





Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		200	V
V_{GS}	Gate-Source Voltage		± 30	V
I_D	Drain Current	T_C = 25℃	50	A
		T_C = 100℃	31.6	A
I_{DM}	Pulsed Drain Current		200	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1333	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	19.8	mJ
I_{AR}	Repetitive Avalanche current	(Note 1)	50	A
P_D	Power Dissipation (T_C = 25℃)		175	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	--	0.71	℃/W
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient	--	62.5	℃/W

Electrical Characteristics T_C=25 ℃ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D =25A	--	0.043	0.051	Ω
R_g	Internal gate resistance	Open drain, f=1MHz	--	1	--	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	200	--	--	V
I_{DSS}	Drain-source cut-off current	V_{DS} = 200 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 160 V, T_C = 125℃	--	--	100	uA
I_{GSSF}	Gate-Body Leakage Current,Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current,Reverse	V_{GS} =- 30 V, V_{DS} = 0 V	--	--	-100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	3800	--	pF
C_{oss}	Output Capacitance		--	480	--	pF
C_{rss}	Reverse Transfer Capacitance		--	64	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 100V, I_D = 50 A, R_G = 25 Ω (Note 4)	--	57	--	ns
t_r	Turn-On Rise Time		--	28	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	169	--	ns
t_f	Turn-Off Fall Time		--	44	--	ns
Q_g	Total Gate Charge	V_{DS} =160 V, I_D =50A, V_{GS} = 10 V (Note 3,4)	--	80	--	nC
Q_{gs}	Gate-Source Charge		--	18.5	--	nC
Q_{gd}	Gate-Drain Charge		--	25.5	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	50	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	200	
V_{SD}	Source-Drain Diode Forward Voltage	I_S =50A, V_{GS} = 0 V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S =50, V_{GS} = 0 V di_F/dt = -100 A/μs (Note 3，4)	--	282	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.3	--	uC

NOTES:

1. Repeated rating: Pulse width limited by safe operating area
2. L=0.8mH, I_{AS}=50A, V_{DD}=50V, R_G=25Ω,Starting T_J=25 ℃
3. Pulse test: Pulse width≤300us, Duty cycle≤2%
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Fig. 1 I_D - V_{DS}

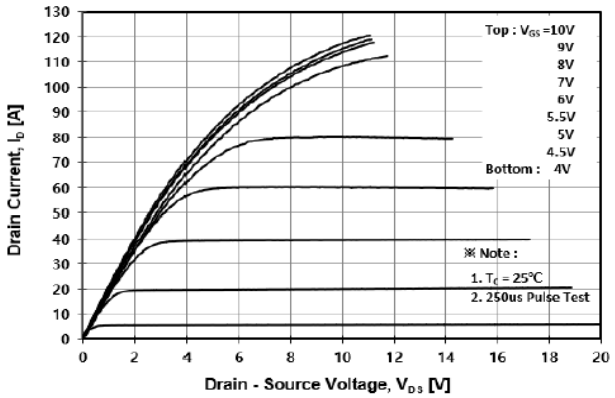


Fig. 2 I_D - V_{GS}

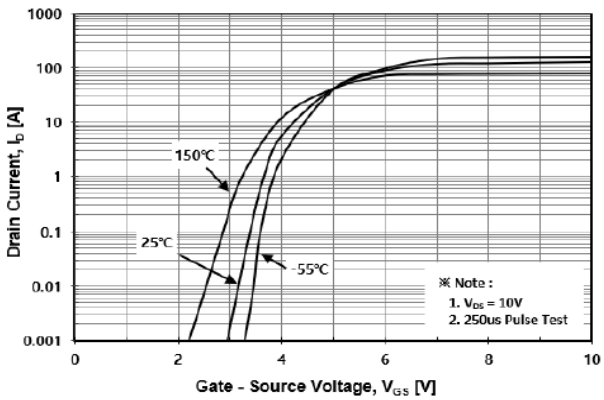


Fig. 3 $R_{DS(ON)}$ - I_D

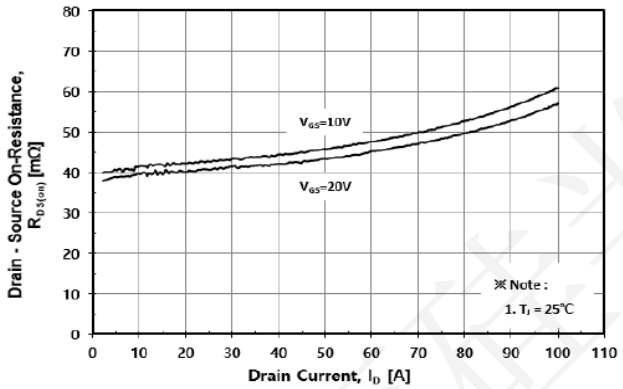


Fig. 4 I_S - V_{SD}

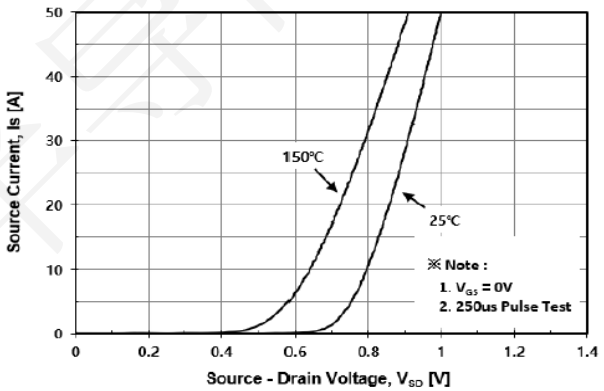


Fig. 5 Capacitance - V_{DS}

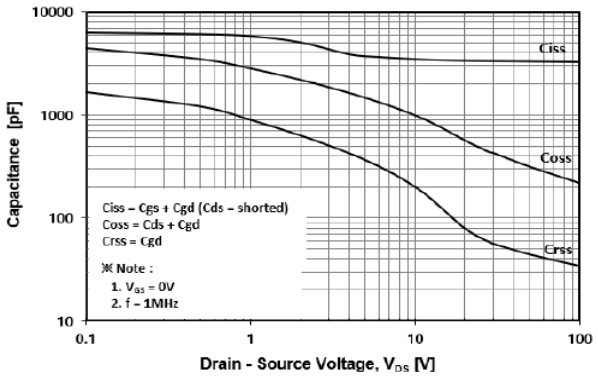
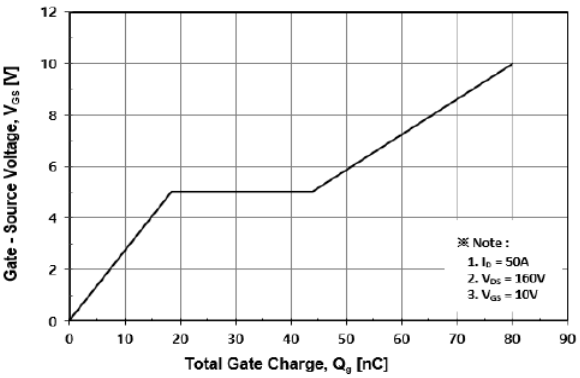


Fig. 6 V_{GS} - Q_G



Typical Characteristics Curve (Continue)

Fig. 7 BV_{DSS} - T_J

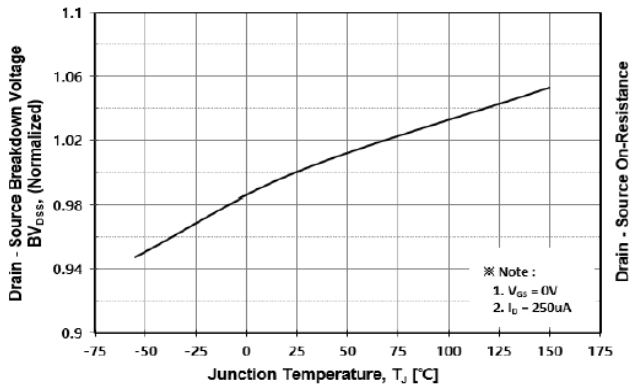


Fig. 8 $R_{DS(ON)}$ - T_J

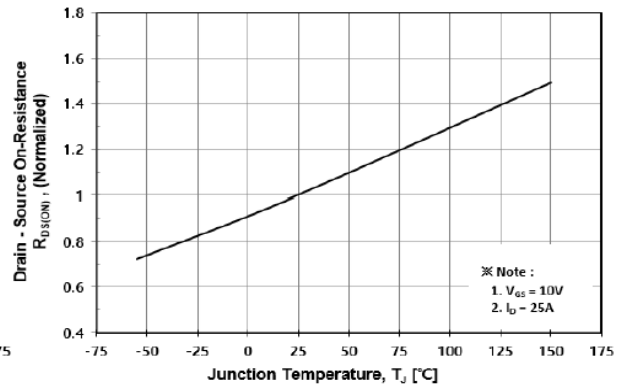


Fig. 9 I_D - T_C

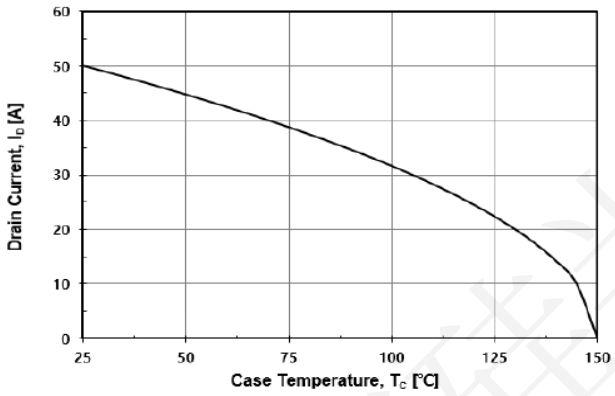


Fig. 10 Safe Operating Area

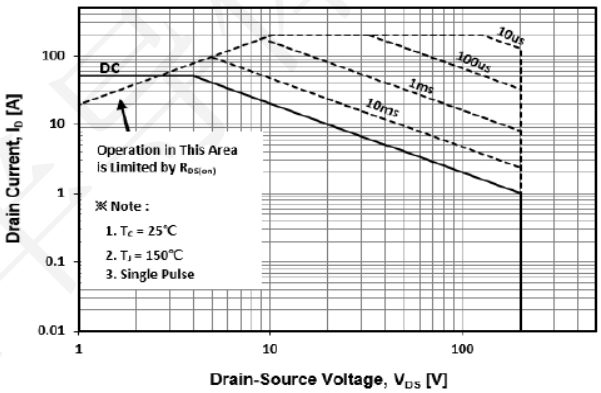


Fig. 11 Transient Thermal Impedance

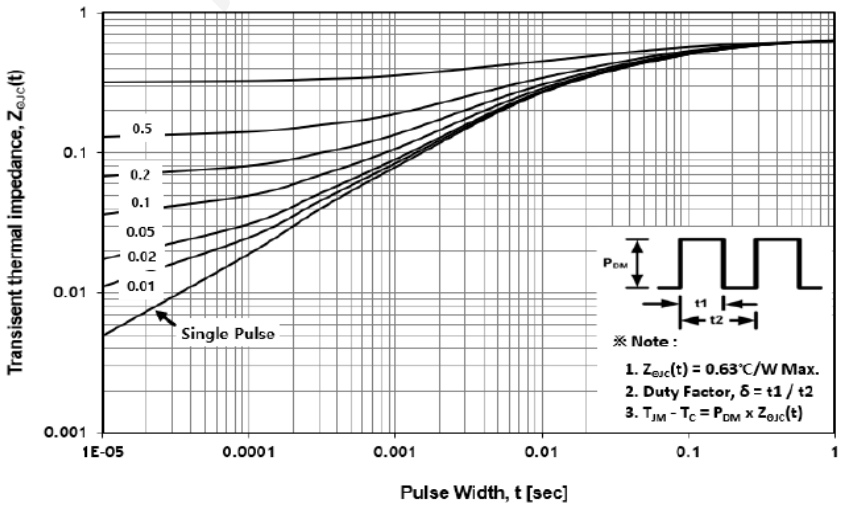
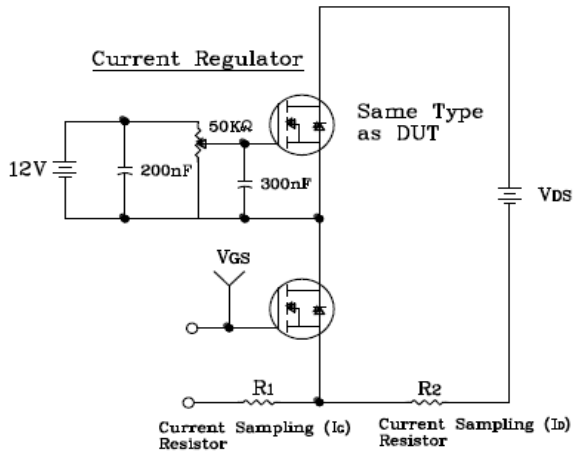


Fig. 12 Gate Charge Test Circuit & Waveform



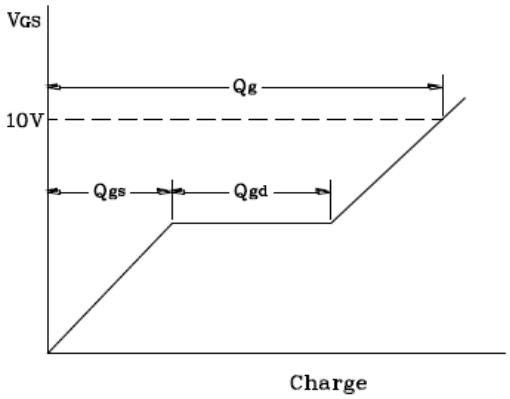
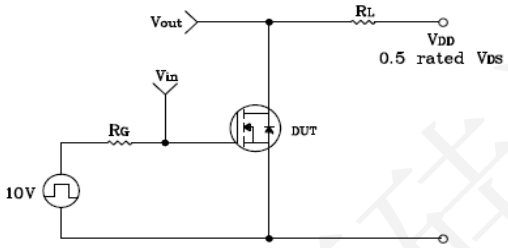


Fig. 13 Resistive Switching Test Circuit & Waveform



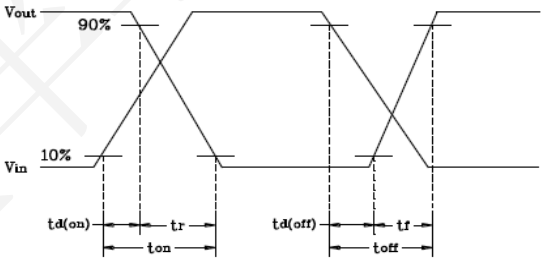
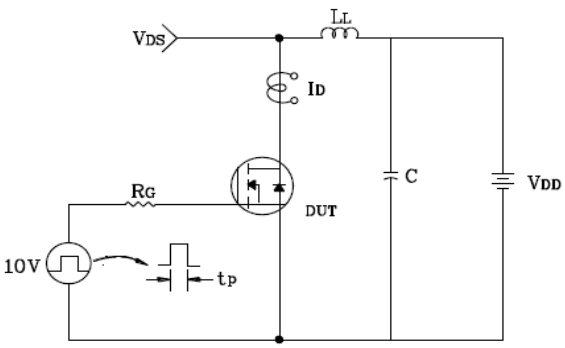


Fig. 14 E_{AS} Test Circuit & Waveform



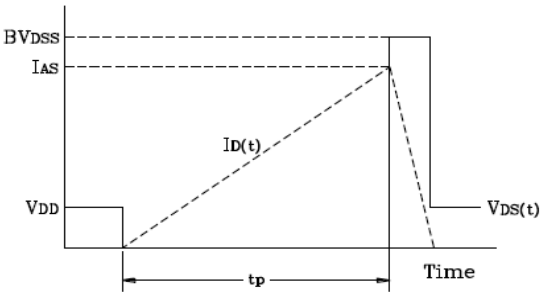


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform