Truesemi®

TSK60N50M

500V N-Channel MOSFET

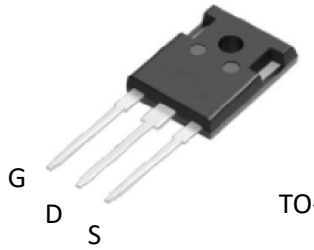
General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Features

60A,500V,Max.RDS(on)=0.095Ω
@ VGS =10V

♦Drain-Source breakdown voltage: BVDSS=500V (Min.)
♦Low drain-source On resistance: RDS(on)=122mΩ (Max.)
♦ 100% avalanche tested
♦ RoHS compliant device



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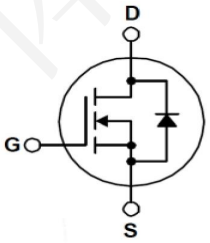


Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		500	V
V_{GS}	Gate-Source Voltage		±30	V
I_D	Drain Current *	T_C = 25℃	60	A
		T_C = 100℃	40	A
I_{DM}	Pulsed Drain Current *		240	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		2569	mJ
I_{AR}	Repetitive avalanche current (Note 2)		68	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		100	mJ
P_D	Power Dissipation (T_C = 25℃)		1000	W
T_J	Junction temperature		150	℃
T_{stg}	Storage temperature range		-55~150	℃

* Limited only maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	--	0.125	℃/W
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient	--	62.5	℃/W

Electrical Characteristics T_C=25 ℃ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 30A	--	0.088	0.095	Ω
R_g	Internal gate resistance	Open drain, f=1MHz	--	0.8	--	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	500	--	--	V
I_{DSS}	Drain-source cut-off current	V_{DS} =500V, V_{GS} = 0 V	--	--	25	uA
		V_{DS}=500V, T_c=125℃	--	--	100	uA
I_{GSS}	Gate leakage current	V_{DS}=0V, V_{GS}=±20V	--	--	±250	Na
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	9592	--	pF
C_{oss}	Output Capacitance		--	728	--	pF
C_{rss}	Reverse Transfer Capacitance		--	68	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time (Note 3,4)	V_{DD} =250 V, I_D =60A, R_G = 25 Ω	--	102	--	ns
t_r	Turn-On Rise Time (Note 3,4)		--	56	--	ns
$t_{d(off)}$	Turn-Off Delay Time (Note 4,5)		--	476	--	ns
t_f	Turn-Off Fall Time (Note 3,4)		--	79	--	ns
Q_g	Total Gate Charge (Note 3,4)	V_{DS} =400V, I_D =60A, V_{GS} = 10 V	--	193	--	nC
Q_{gs}	Gate-Source Charge (Note 3,4)		--	43	--	nC
Q_{gd}	Gate-Drain Charge (Note 3,4)		--	63	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	60	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	240	
V_{SD}	Source-Drain Diode Forward Voltage	I_S =60A, V_{GS} = 0 V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S =50A, V_{GS} = 0 V, di_F/dt = 100 A/μs (Note 3, 4)	--	602	--	ns
Q_{rr}	Reverse Recovery Charge		--	6.35	--	uC

NOTES:

1. Repeated rating: Pulse width limited by safe operating area
2. L=1mH, I_{AS}=68A, V_{DD}=50V, R_G=25Ω, Starting TJ=25℃
3. Pulse test: Pulse width≤300us, Duty cycle≤2%
4. Essentially independent of operating temperature typical characteristics

Typical Characteristics Curve

Fig. 1 Typical Output Characteristics

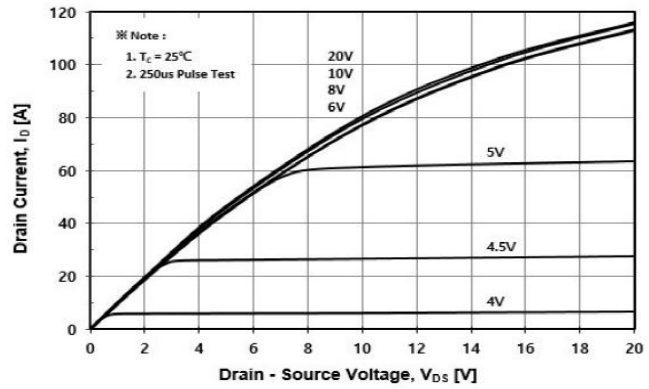


Fig. 2 Typical Transfer Characteristics

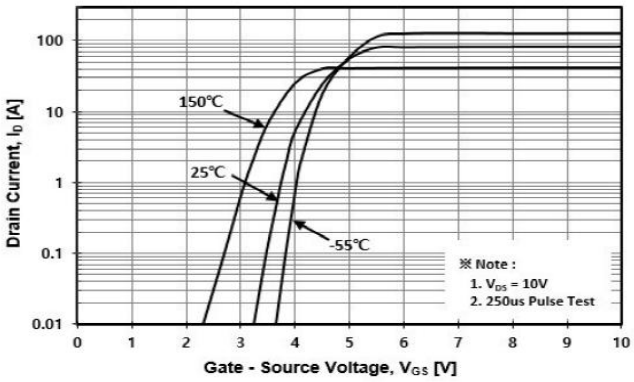


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

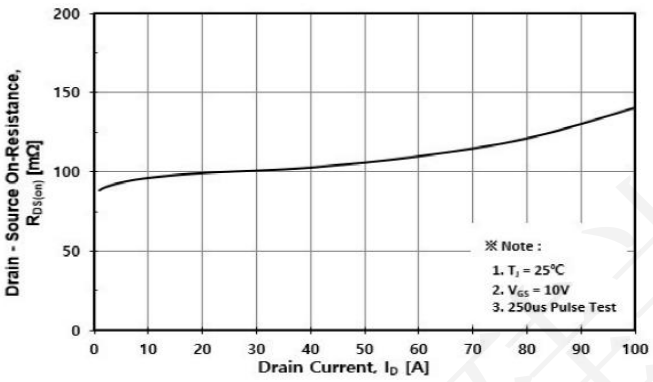


Fig. 4 Body Diode Forward Voltage Variation with Source Current

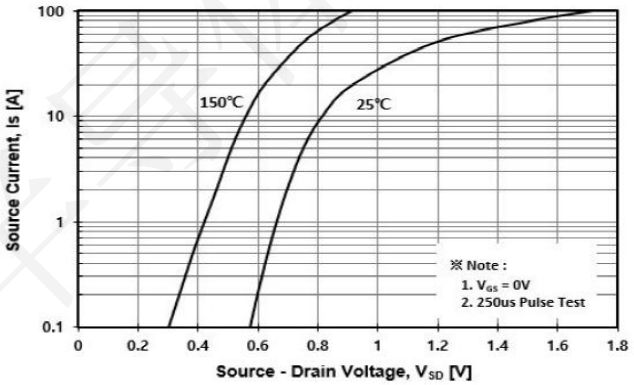


Fig. 5 Typical Capacitance Characteristics

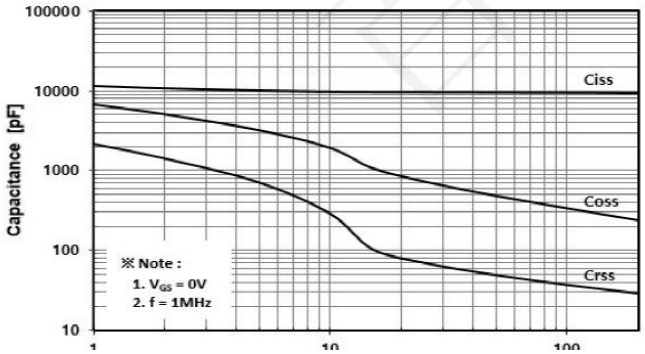
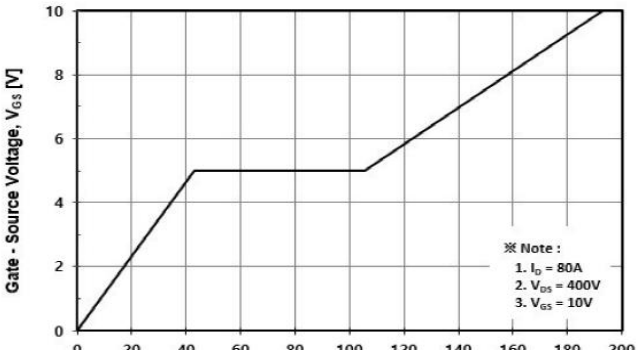


Fig. 6 Typical Total Gate Charge Characteristics



Typical Characteristics Curve (Continue)

Fig. 7 Breakdown Voltage Variation vs. Temperature

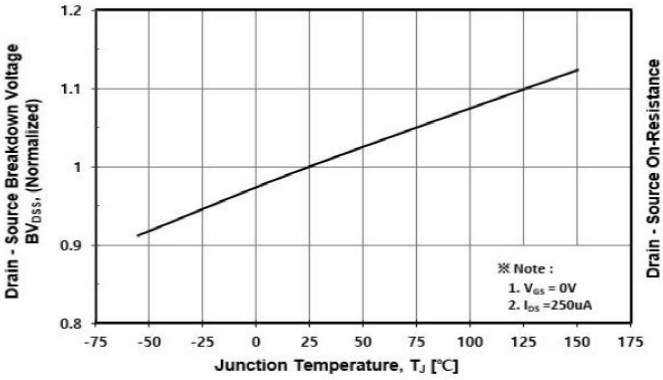


Fig. 8 On-Resistance Variation vs. Temperature

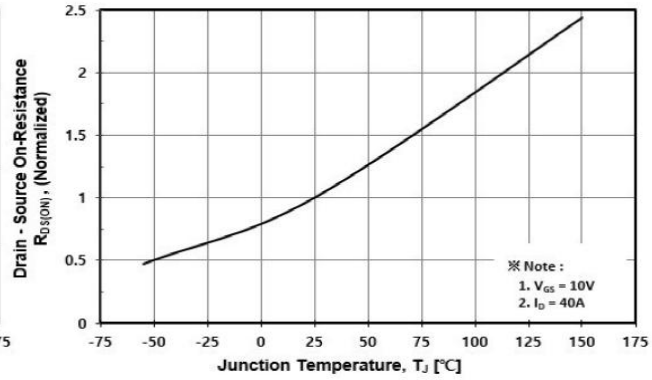


Fig. 9 Maximum Drain Current vs. Case Temperature

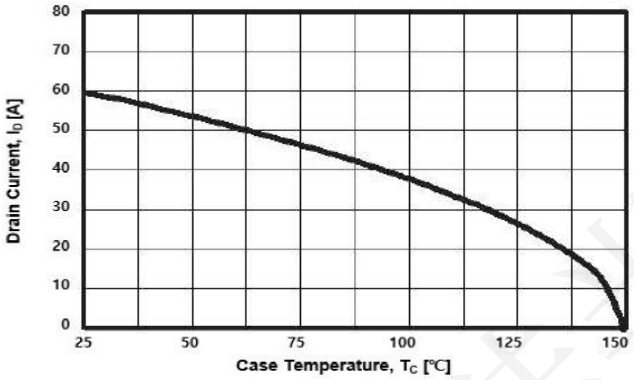


Fig. 10 Maximum Safe Operating Area

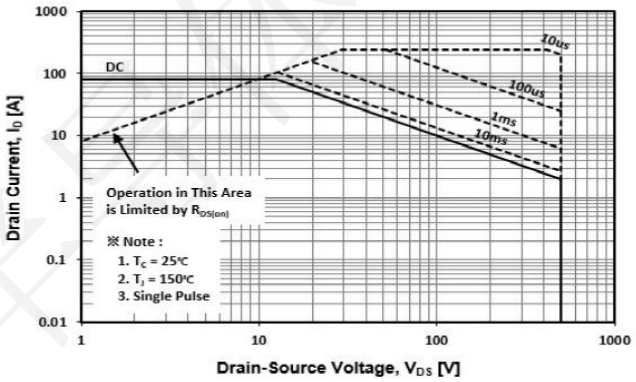


Fig. 11 Transient Thermal Impedance

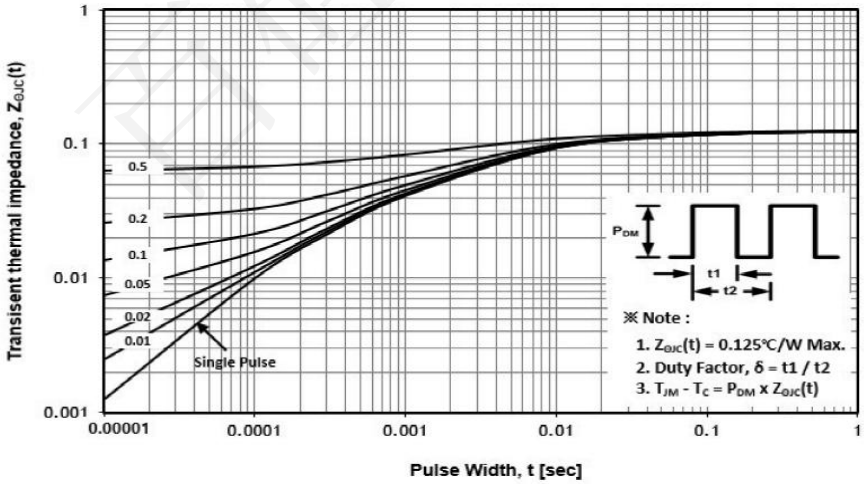
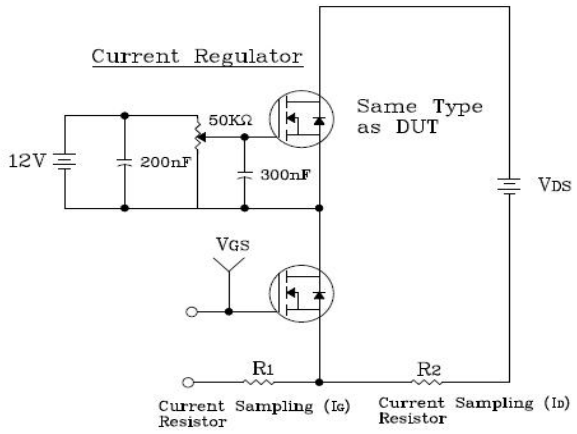


Fig. 12 Gate Charge Test Circuit & Waveform



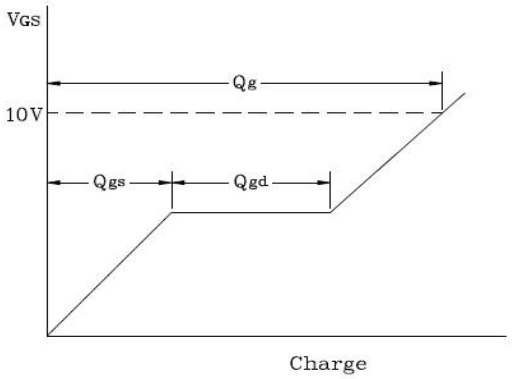
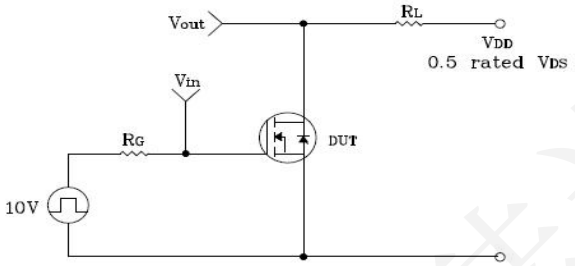


Fig. 13 Resistive Switching Test Circuit & Waveform



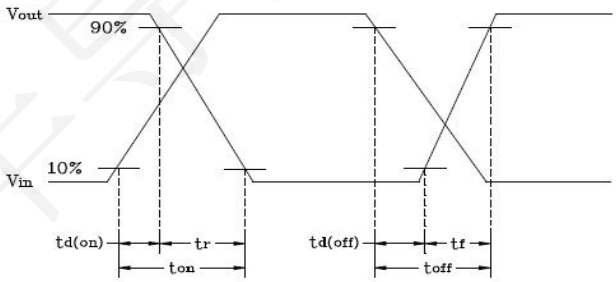
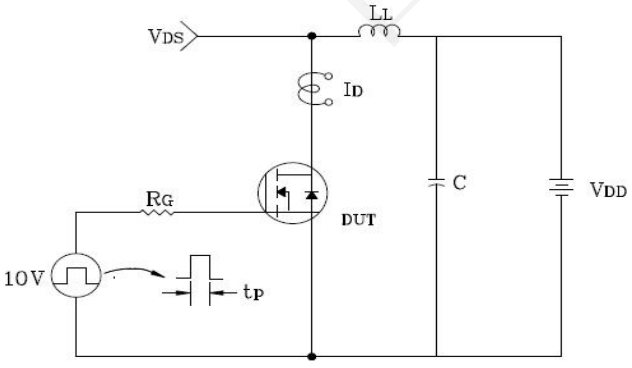


Fig. 14 E_{AS} Test Circuit & Waveform



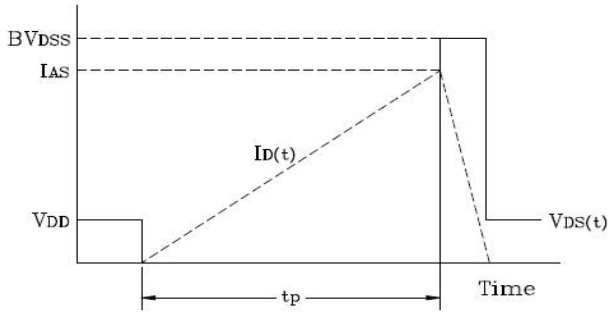


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform