Truesemi®

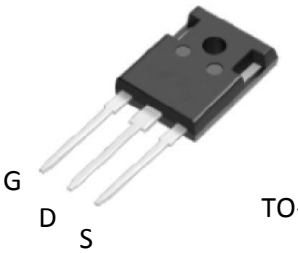
# TSK50N30M

## 300V N-Channel MOSFET

### Features

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

- 50A,300V,Max.RDS(on)=0.06Ω @ VGS =10V
- Drain-Source breakdown voltage: BVDSS=300V (Min.)
- Low gate charge: Qg=122nC (Typ.)
- 100% avalanche tested
- RoHS compliant device

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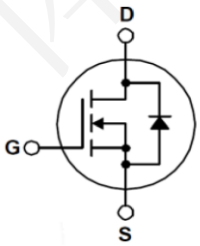



### Absolute Maximum Ratings

$T_C$=25℃ unless otherwise specified

| Symbol | Parameter | | Value | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 300 | V |
| $V_{GS}$ | Gate-Source Voltage | | ± 30 | V |
| $I_D$ | Drain Current | $T_C$ = 25℃ | 50 | A |
| | | $T_C$ = 100℃ | 31 | A |
| $I_{DM}$ | Pulsed Drain Current | (Note 1) | 200 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 1875 | mJ |
| $I_{AS}$ | Single avalanche current | (Note 2) | 25 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 19.80 | mJ |
| $P_D$ | Power Dissipation ($T_C$ = 25℃) | | 198 | W |
| $T_J$ | Junction temperature | | 150 | ℃ |
| $T_{stg}$ | Storage temperature range | | -55~150 | ℃ |

### Thermal Resistance Characteristics

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance,Junction-to-Case | -- | 0.63 | ℃/W |
| $R_{\theta JA}$ | Thermal Resistance,Junction-to-Ambient | -- | 62.5 | ℃/W |

## Electrical Characteristics $T_C$=25 ℃ unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 uA | 2.0 | -- | 4.0 | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 25A | -- | 0.05 | 0.06 | Ω |
| $R_g$ | Internal gate resistance | Open drain, f=1MHz | -- | 1 | -- | Ω |
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 uA | 300 | -- | -- | V |
| $I_{DSS}$ | Drain-source cut-off current | $V_{DS}$ = 300 V, $V_{GS}$ = 0 V | -- | -- | 1 | uA |
| | | $V_{DS}$=300V, $T_c$=125 C | -- | -- | 100 | uA |
| $I_{GSS}$ | Gate leakage current | $V_{DS}$=0V, $V_{GS}$=±30V | -- | -- | ±100 | Na |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 5490 | -- | pF |
| $C_{oss}$ | Output Capacitance | | -- | 600 | -- | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 65 | -- | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Time (Note 3,4) | $V_{DD}$ = 150 V, $I_D$ = 50 A, $R_G$ = 25 Ω | -- | 71 | -- | ns |
| $t_r$ | Turn-On Rise Time (Note 3,4) | | -- | 35 | -- | ns |
| $t_{d(off)}$ | Turn-Off Delay Time (Note 4,5) | | -- | 324 | -- | ns |
| $t_f$ | Turn-Off Fall Time (Note 3,4) | | -- | 51 | -- | ns |
| $Q_g$ | Total Gate Charge (Note 3,4) | $V_{DS}$ =240 V, $I_D$ = 50A, $V_{GS}$ = 10 V | -- | 122 | -- | nC |
| $Q_{gs}$ | Gate-Source Charge (Note 3,4) | | -- | 28 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge (Note 3,4) | | -- | 42 | -- | nC |
| **Source-Drain Diode Maximum Ratings and Characteristics** | | | | | | |
| $I_S$ | Continuous Source-Drain Diode Forward Current | | -- | -- | 50 | A |
| $I_{SM}$ | Pulsed Source-Drain Diode Forward Current | | -- | -- | 200 | A |
| $V_{SD}$ | Source-Drain Diode Forward Voltage | $I_S$ = 50A, $V_{GS}$ = 0 V | -- | -- | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_S$ = 50A, $V_{GS}$ = 0 V, $di_F/dt$ = 100 A/μs (Note 3, 4) | -- | 318 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 3.4 | -- | uC |

**NOTES:**

1. Repeated rating: Pulse width limited by safe operating area
2. L=5mH, IAS=25A, VDD=50V, RG=25Ω, Starting TJ=25 C
3. Pulse test: Pulse width≤300us, Duty cycle≤2%
4. Essentially independent of operating temperature typical characteristics

## Typical Characteristics Curve

Fig. 1 $I_D$ - $V_{DS}$

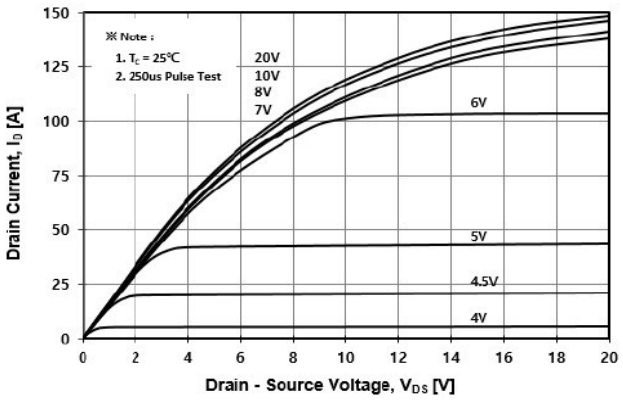



Fig. 2 $I_D$ - $V_{GS}$

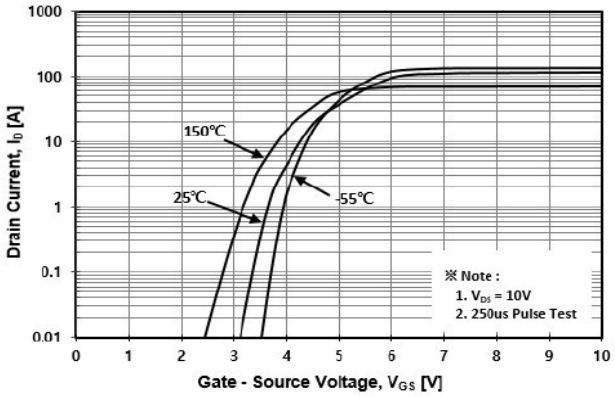



Fig. 3 $R_{DS(ON)}$ - $I_D$

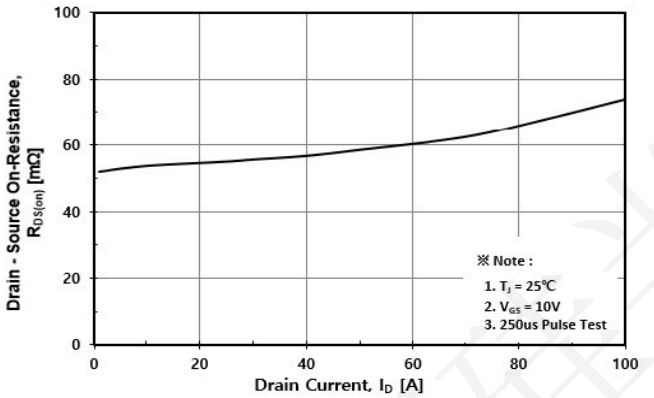



Fig. 4 $I_S$ - $V_{SD}$

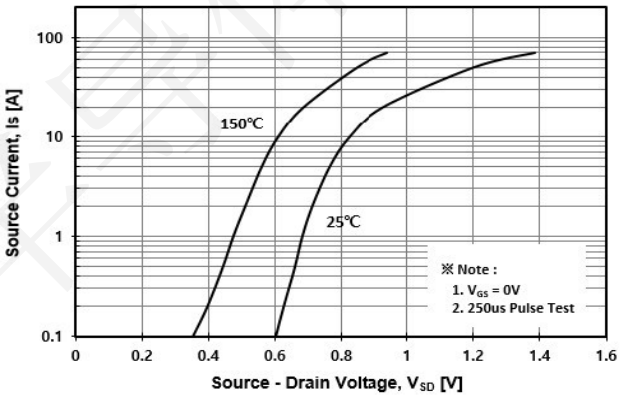



Fig. 5 Capacitance - $V_{DS}$

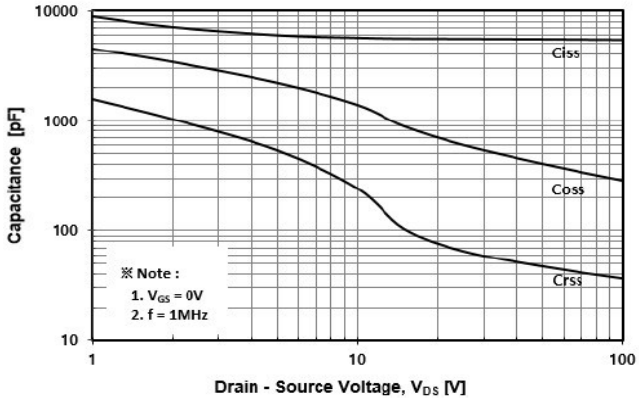
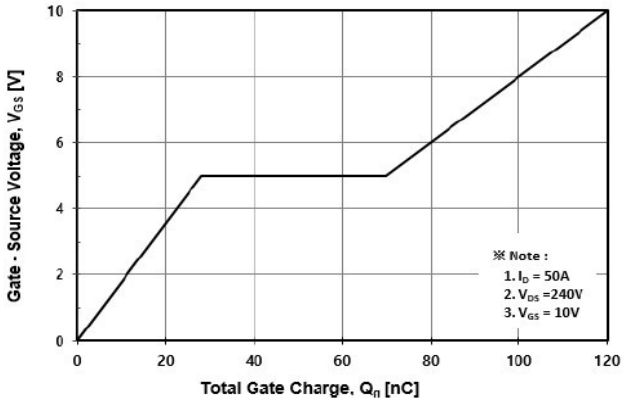



Fig. 6 $V_{GS}$ - $Q_G$



## Typical Characteristics Curve (Continue)

Fig. 7 $BV_{DSS}$ - $T_J$

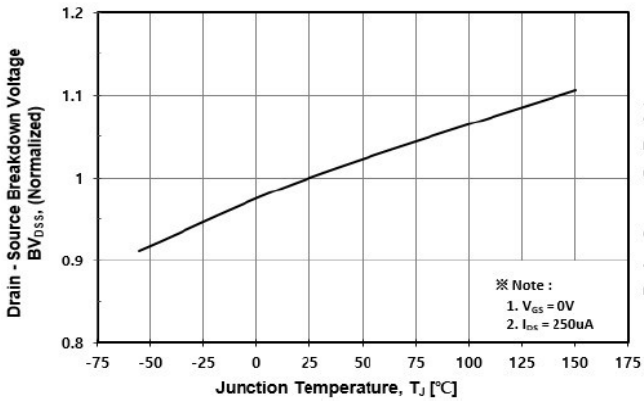



Fig. 8 $R_{DS(ON)}$ - $T_J$

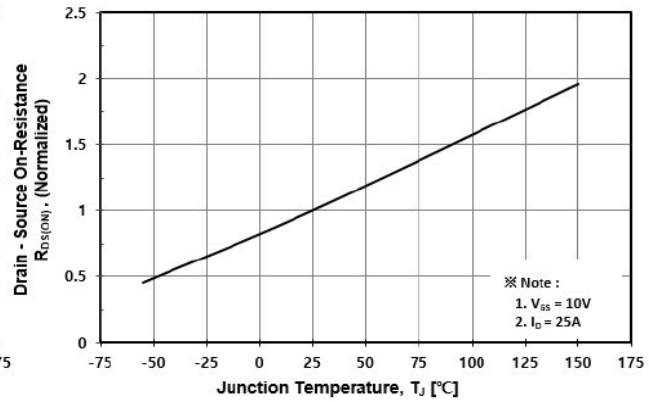



Fig. 9 $I_D$ - $T_C$

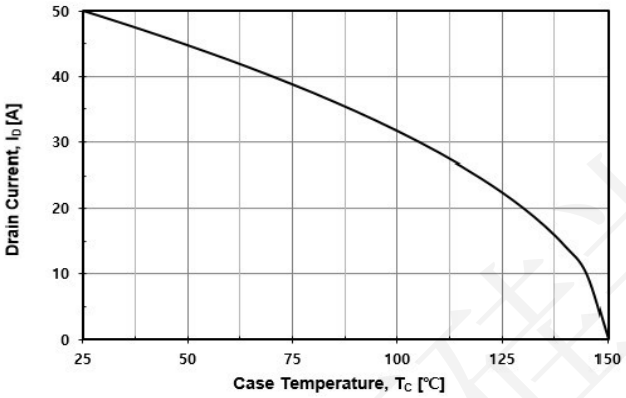



Fig. 10 Safe Operating Area

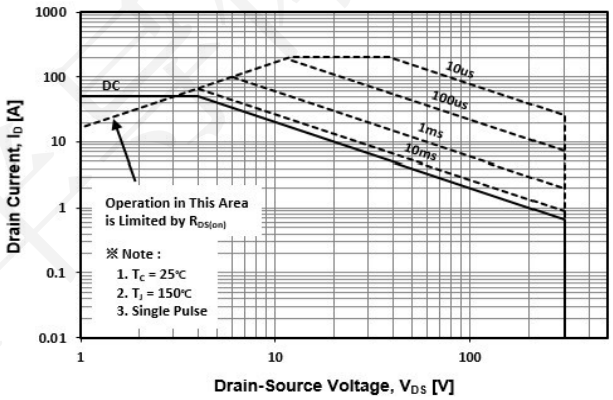
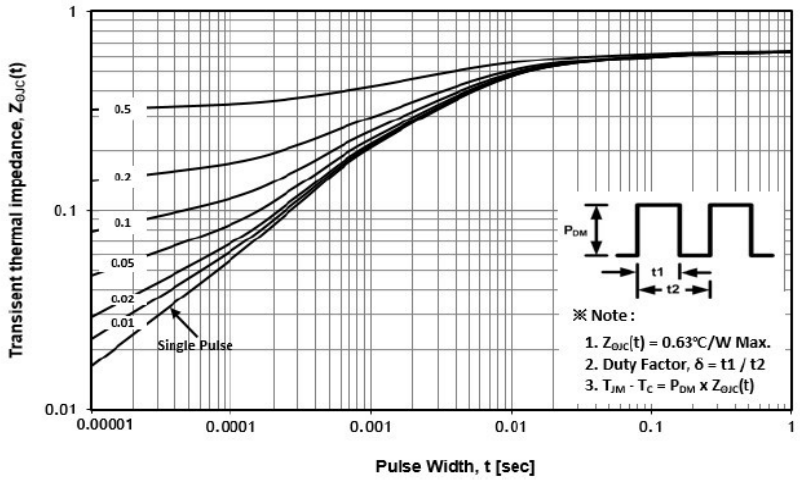
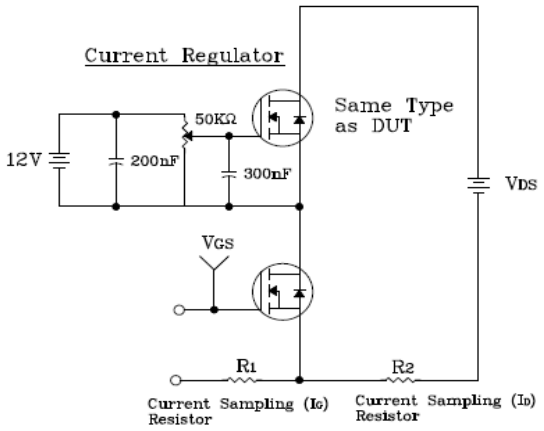
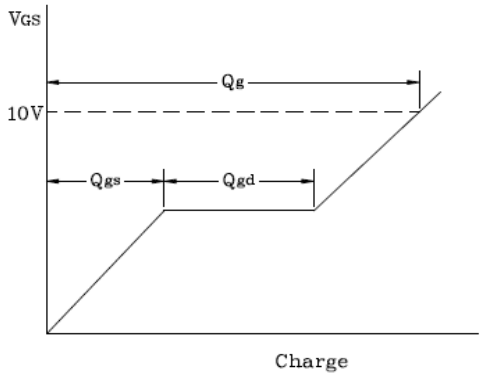



Fig. 11 Transient Thermal Impedance

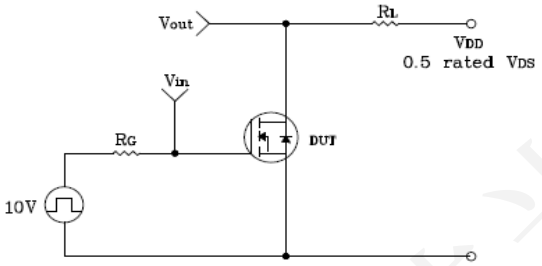


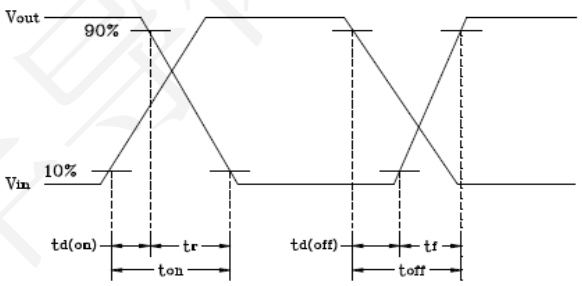
## Fig. 12 Gate Charge Test Circuit & Waveform



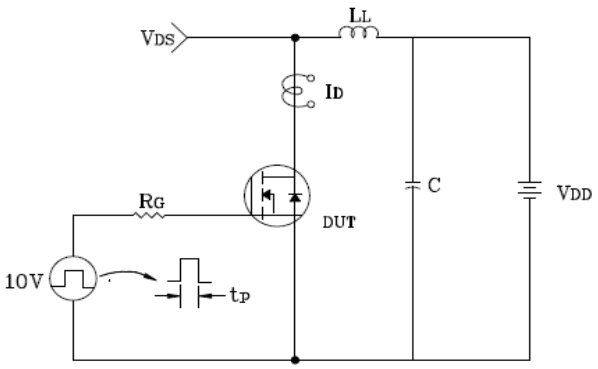



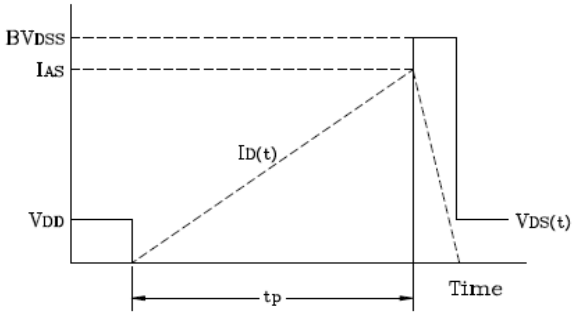

## Fig. 13 Resistive Switching Test Circuit & Waveform




## Fig. 14 $E_{AS}$ Test Circuit & Waveform



## Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform