



# TSP7N80M/TSF7N80M

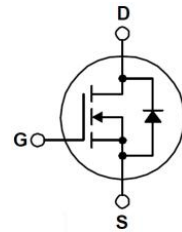
## 800V N-Channel MOSFET

### General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

### Features

- 7.0A,800V,Max. $R_{DS(on)}=1.9\ \Omega$  @  $V_{GS}=10V$
- Low gate charge(typical 40nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	TSP7N80M	TSF7N80M	Units	
$V_{DSS}$	Drain-Source Voltage	800		V	
$V_{GS}$	Gate-Source Voltage	$\pm 30$		V	
$I_D$	Drain Current	$T_C = 25^\circ\text{C}$	7.0	7.0*	A
		$T_C = 100^\circ\text{C}$	4.2	4.2*	A
$I_{DM}$	Pulsed Drain Current (Note 1)	28	28*	A	
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	650		mJ	
$I_{AR}$	Avalanche Current (Note 1)	7.0		A	
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	16.7		mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns	
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) -Derate above $25^\circ\text{C}$	167	56	W	
		1.33	0.44	W/ $^\circ\text{C}$	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$	
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$	

\* Drain current limited by maximum junction temperature.

### Thermal Resistance Characteristics

Symbol	Parameter	TSP7N80M	TSF7N80M	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.75	2.25	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

**Electrical Characteristics**  $T_J=25\text{ }^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**On Characteristics**

$V_{GS}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$	--	1.4	1.9	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=40\text{V}, I_D=3.5\text{A}$ (Note 4)	--	5.7	--	S

**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	800	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$	--	0.8	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 640\text{ V}, T_J = 125\text{ }^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1685	--	pF
$C_{oss}$	Output Capacitance		--	165	--	pF
$C_{riss}$	Reverse Transfer Capacitance		--	17	--	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Time	$V_{DS} = 400\text{ V}, I_D = 7.0\text{ A},$ $R_G = 25\text{ }\Omega$  (Note 4,5)	--	40	--	ns
$t_r$	Turn-On Rise Time		--	100	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	50	--	ns
$t_f$	Turn-Off Fall Time		--	60	--	ns
$Q_g$	Total Gate Charge	$V_{DS} = 640\text{ V}, I_D = 7.0\text{ A},$ $V_{GS} = 10\text{ V}$  (Note 4,5)	--	40	--	nC
$Q_{gs}$	Gate-Source Charge		--	9.0	--	nC
$Q_{gd}$	Gate-Drain Charge		--	16.5	--	nC

**Source-Drain Diode Maximum Ratings and Characteristics**

$I_S$	Continuous Source-Drain Diode Forward Current	--	--	7.0	A	
$I_{SM}$	Pulsed Source-Drain Diode Forward Current	--	--	28		
$V_{SD}$	Source-Drain Diode Forward Voltage	$I_S = 7.0\text{ A}, V_{GS} = 0\text{ V}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$I_S = 7.0\text{ A}, V_{GS} = 0\text{ V}$	--	765	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	6.8	--	$\mu\text{C}$

**NOTES:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L=25\text{mH}, I_{AS}=7.0\text{A}, V_{DD}=50\text{V}, R_G=25\text{ }\Omega$ , Starting  $T_J=25\text{ }^\circ\text{C}$
3.  $I_{SP} \leq 7.0\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25\text{ }^\circ\text{C}$
4. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

# Typical Characteristics

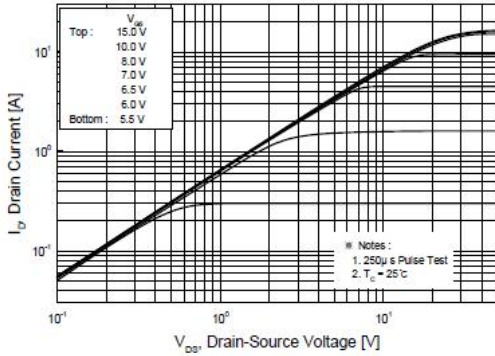


Figure 1. On-Region Characteristics

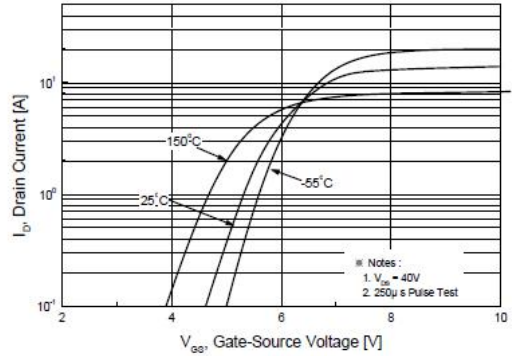


Figure 2. Transfer Characteristics

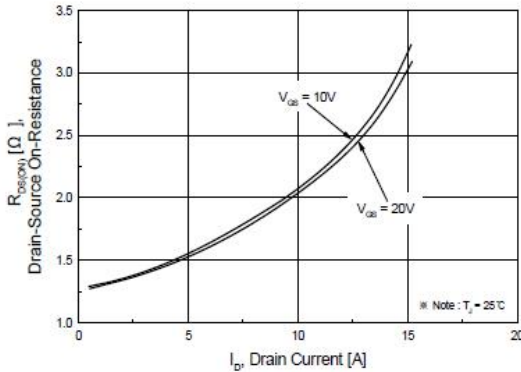


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

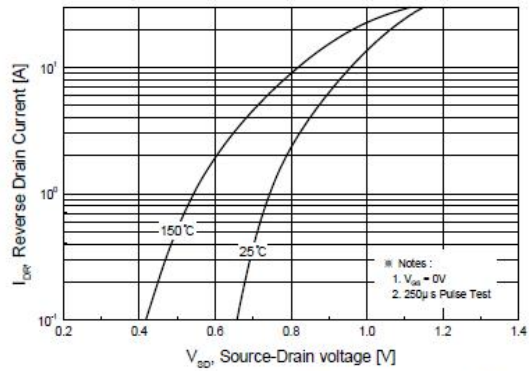


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

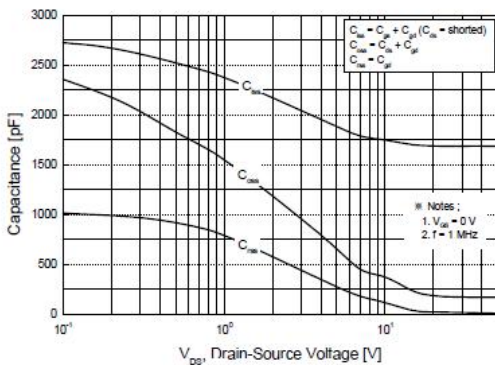


Figure 5. Capacitance Characteristics

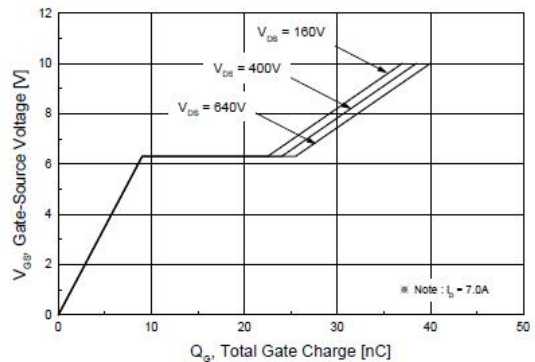


Figure 6. Gate Charge Characteristics

Typical Characteristics

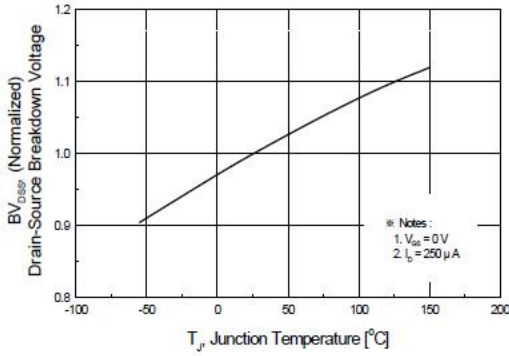


Figure 7. Breakdown Voltage Variation vs Temperature

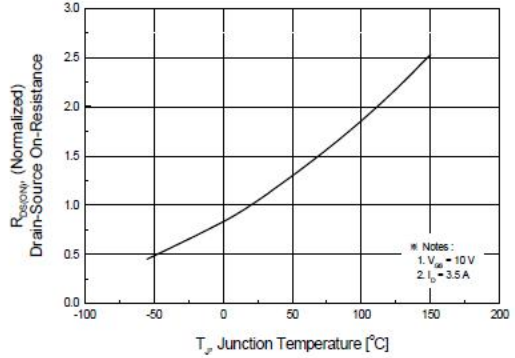


Figure 8. On-Resistance Variation vs Temperature

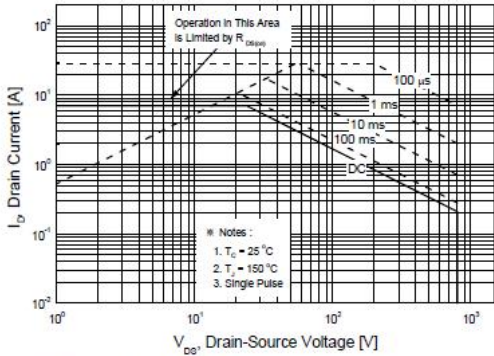


Figure 9-1. Maximum Safe Operating Area for TSP7N80M

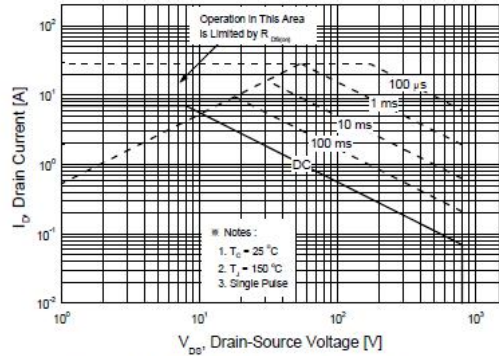


Figure 9-2. Maximum Safe Operating Area for TSF7N80M

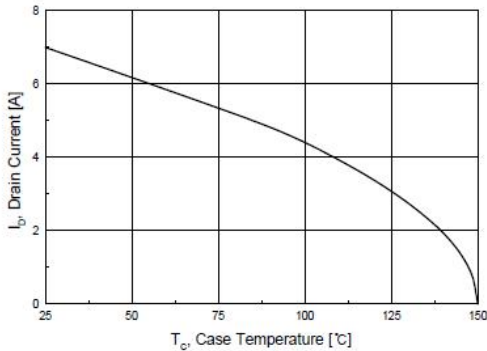


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics

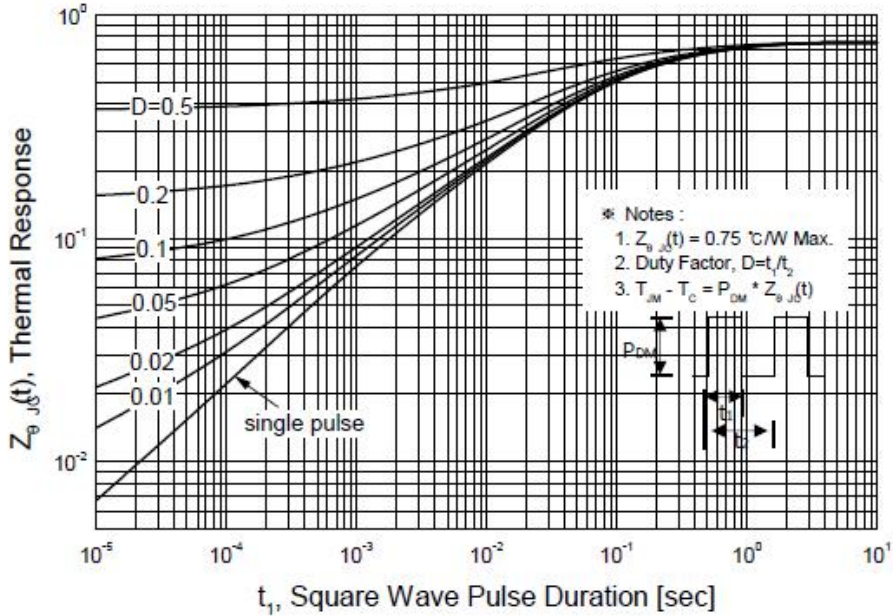


Figure 11-1. Transient Thermal Response Curve for TSP7N80M

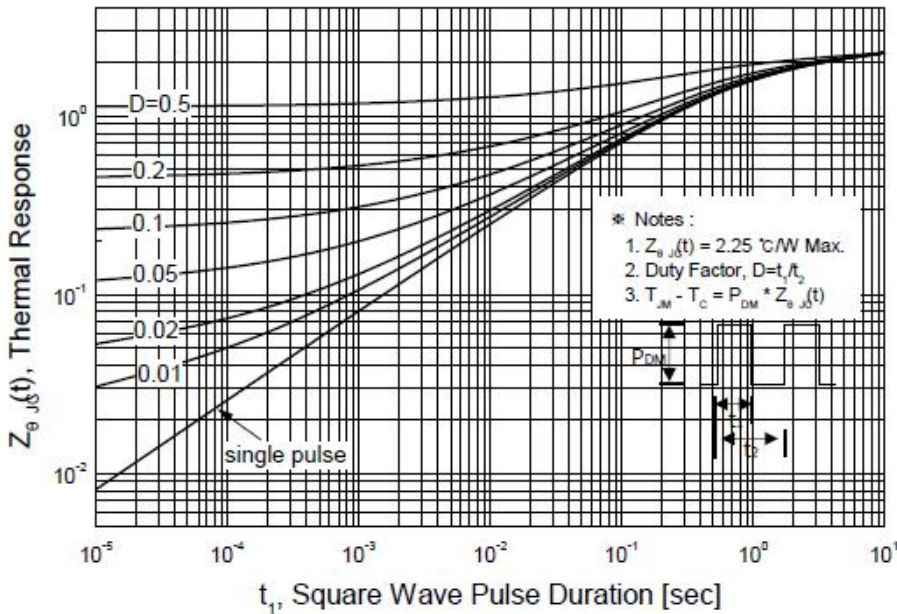


Figure 11-2. Transient Thermal Response Curve for TSF7N80M

Fig 12. Gate Charge Test Circuit & Waveform

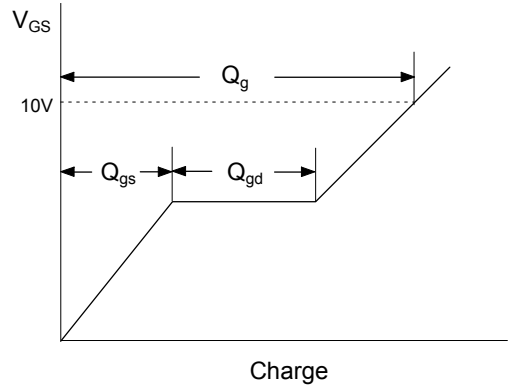
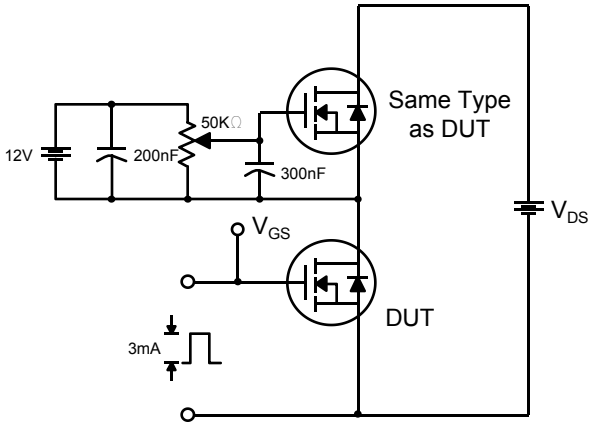


Fig 13. Resistive Switching Test Circuit & Waveforms

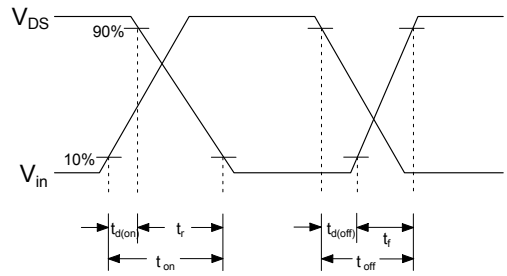
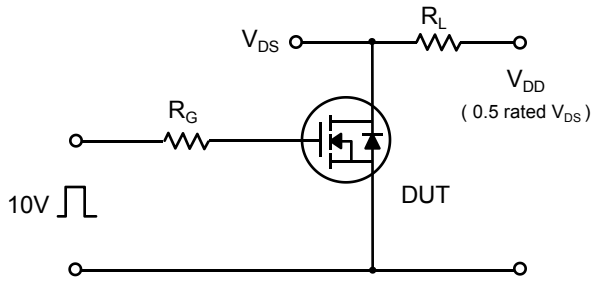


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

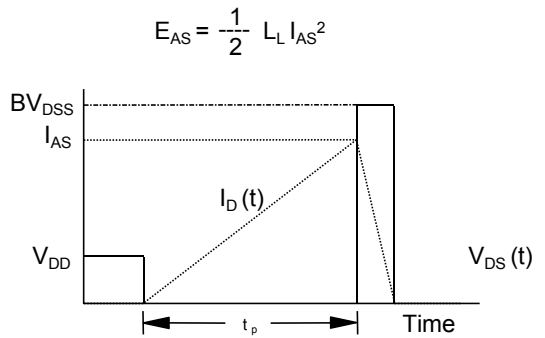
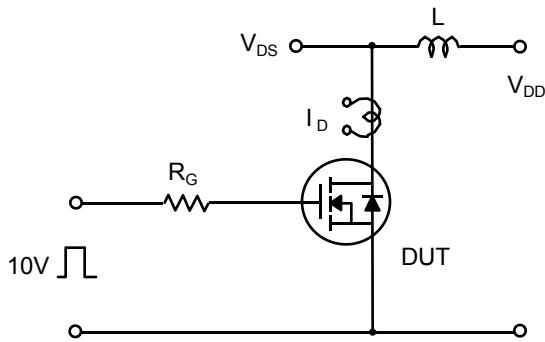
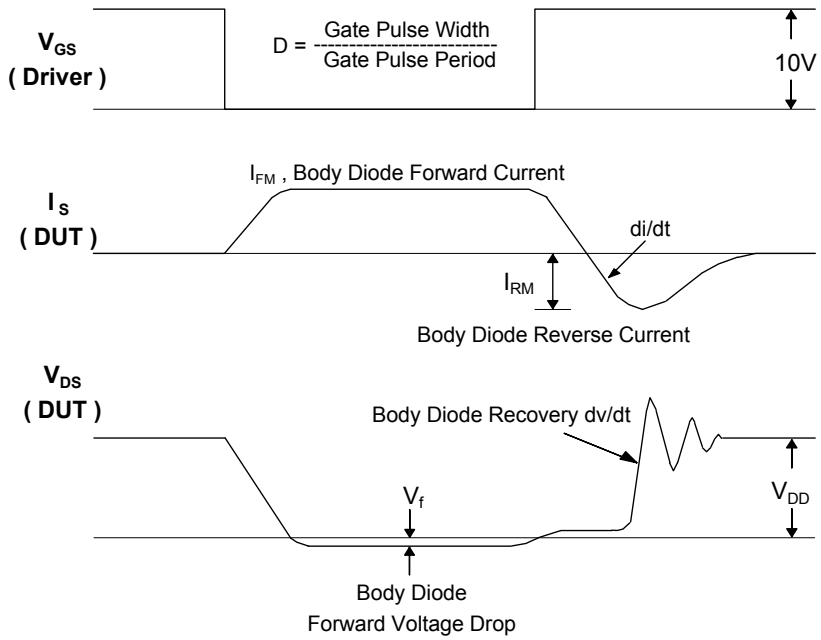
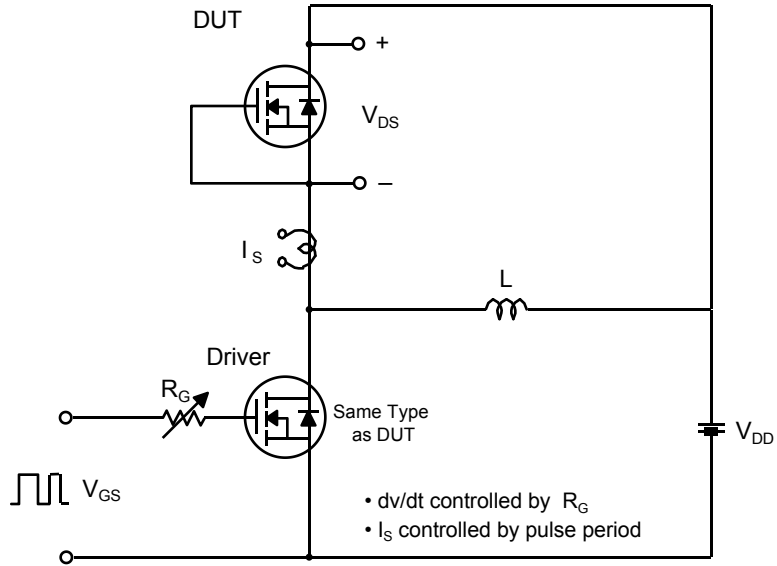
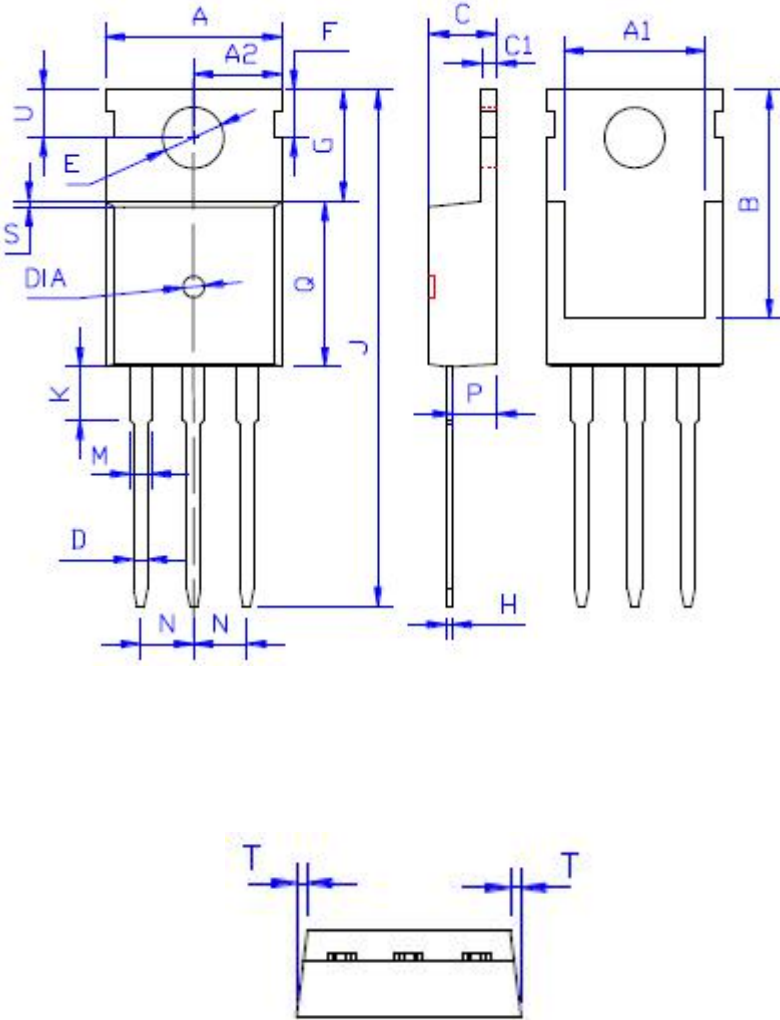


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

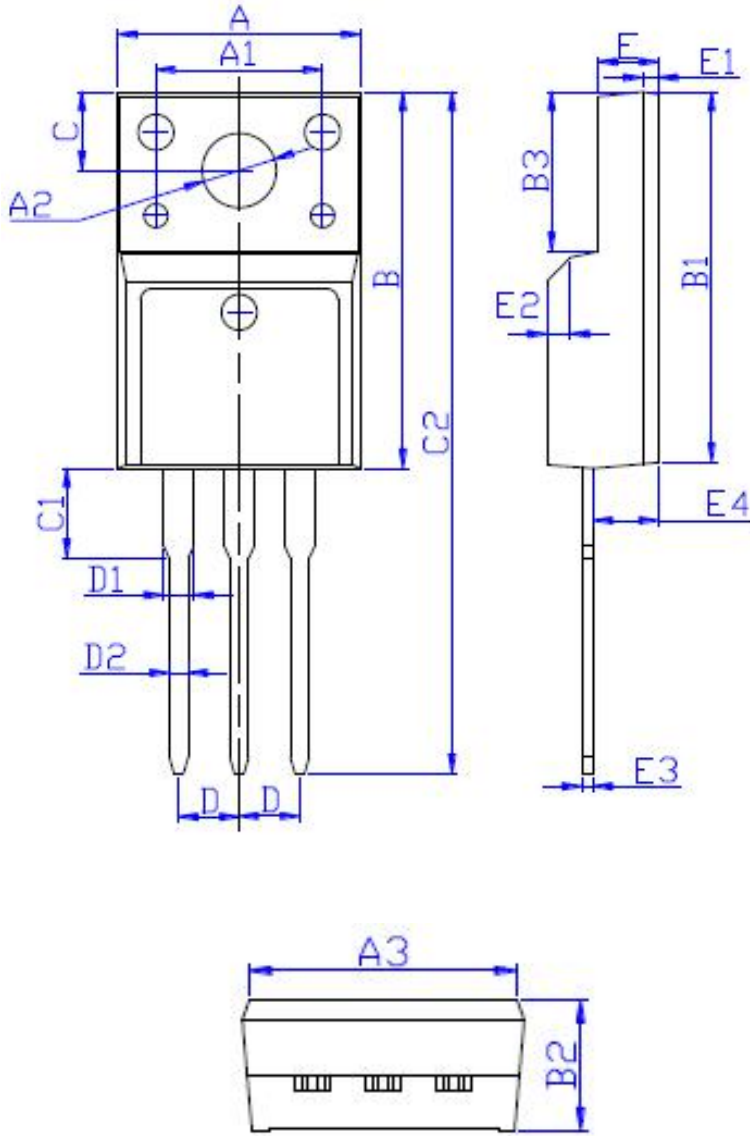
TO-220



DIM	MILLIMETERS
A	10.00±0.30
A1	8.00±0.30
A2	5.00±0.30
B	13.20±0.40
C	4.50±0.20
C1	1.30±0.20
D	0.80±0.20
E	3.60±0.20
F	3.00±0.30
G	6.60±0.40
H	0.50±0.20
J	28.88±0.50
K	3.00±0.30
M	1.30±0.30
N	Typical 2.54
P	2.40±0.40
Q	9.20±0.40
S	0.25±0.15
T	0.25±0.15
U	2.80±0.30
DIA	宽 1.50±0.10 深 0.50 MAX

Package Dimension

TO-220F



DIM	MILLIMETERS
A	10.16 ± 0.30
A1	7.00 ± 0.20
A2	3.12 ± 0.20
A3	9.70 ± 0.30
B	15.90 ± 0.50
B1	15.60 ± 0.50
B2	4.70 ± 0.30
B3	6.70 ± 0.30
C	3.30 ± 0.25
C1	3.25 ± 0.30
C2	28.70 ± 0.50
D	Typical 2.54
D1	1.47 (MAX)
D2	0.80 ± 0.20
E	2.55 ± 0.25
E1	0.70 ± 0.25
E2	1.0 × 45°
E3	0.50 ± 0.20
E4	2.75 ± 0.30