



TSF65R140SD

650V N-Channel MOSFET

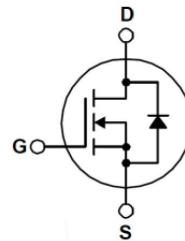
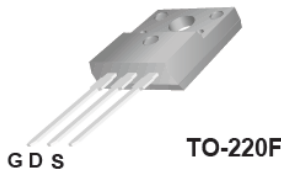
TSF65R140SD

Description

The 65R140 is power MOSFET using Truesemi's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

Features

- 22A,650V,Max.RDS(on)=0.14Ω @ VGS =10V
- Super_Junction technology
- Much lower Ron*A performance for On-state efficiency
- Much lower FOM for fast switching efficiency



Absolute Maximum Ratings Tc=25°C unless otherwise specified

Symbol	Parameter	Value	Units
V _{DSS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	± 30	V
I _D	Drain Current	T _C = 25°C	22
		T _C = 100°C	14
I _{DM}	Pulsed Drain Current (T _C = 25°C, tp limited by T _{jmax})	88	A
E _{AS}	Avalanche energy, single pulse (L=30mH, R _g =30Ω)	300	mJ
P _D	Power Dissipation (T _C = 25°C)	20	W
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C

Thermal Resistance Characteristics

Symbol	Parameter	Value	Units
R _{θJC}	Thermal Resistance,Junction-to-Case.Max	6.23	°C/W
R _{θJA}	Thermal Resistance,Junction-to-Ambient.Max	64	°C/W

Electrical Characteristics $T_c=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 11\text{ A}$	--	0.11	0.14	Ω
g_{fs}	Forward transfer conductance	$V_{DS} = 20\text{ V}, I_D = 11\text{ A}$	--	16.5	--	S

Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	--	--	5	μA
		$V_{DS} = 650\text{ V}, T_c = 150\text{ }^\circ\text{C}$	--	220	--	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1595	--	pF
C_{oss}	Output Capacitance		--	90	--	pF
C_{rss}	Reverse Transfer Capacitance		--	1.6	--	pF

Switching Characteristics						
$t_{d(on)}$	Turn-On Time	$T_j = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V},$ $I_D = 11\text{ A}, V_{DS} = 400\text{ V},$ $R_g = 27\text{ }\Omega$	--	60	--	ns
t_r	Turn-On Rise Time		--	61	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	140	--	ns
t_f	Turn-Off Fall Time		--	31	--	ns
R_G	Gate resistance	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V},$ $f = 1\text{ MHz}$	--	9.8	--	Ω
Q_g	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 480\text{ V},$ $I_D = 11\text{ A}$	--	46	--	nC
Q_{gs}	Gate-Source Charge		--	13.9	--	nC
Q_{gd}	Gate-Drain Charge		--	24	--	nC

Source-Drain Diode Maximum Ratings and Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 11\text{ A}, V_{GS} = 0\text{ V}$	0.6	0.86	1.1	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 11\text{ A}$ $dI/dt = 100\text{ A}/\mu\text{s},$ $V_{DS} = 400\text{ V}$	--	120	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.63	--	μC

Typical Performance Characteristics

Fig 1. Output Characteristics (Tj=25°C)

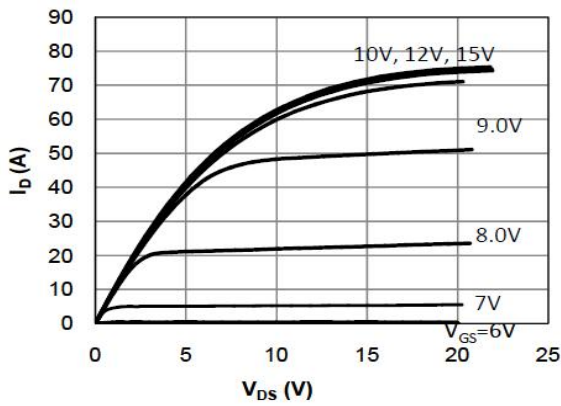


Fig 2. Output Characteristics (Tj=150°C)

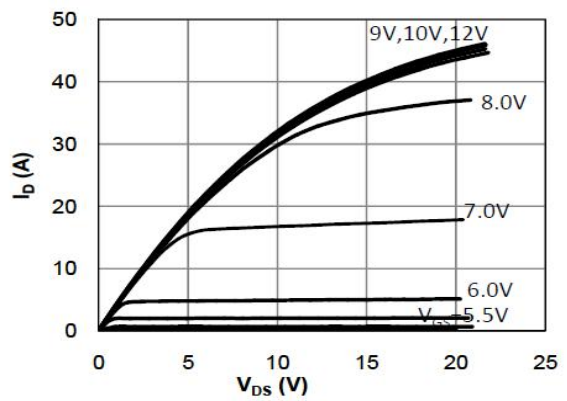


Fig 3: Transfer Characteristics

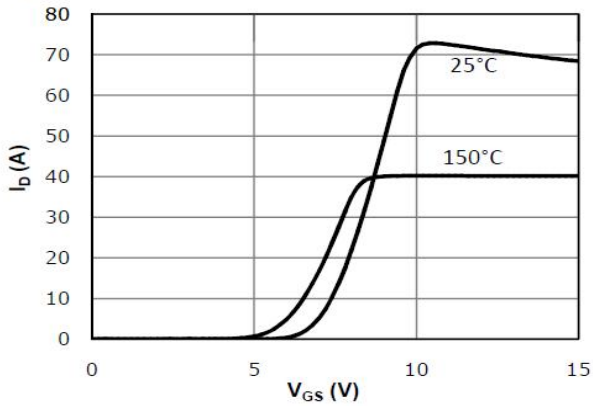


Fig 4: V_{TH} Vs T_j Temperature Characteristics

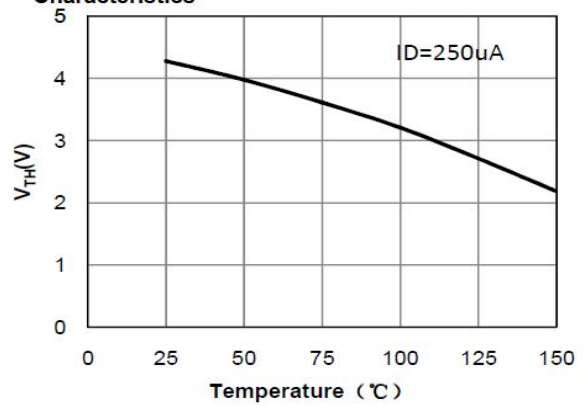


Fig 5: $R_{DS(on)}$ Vs I_D Characteristics ($T_c=25^\circ\text{C}$)

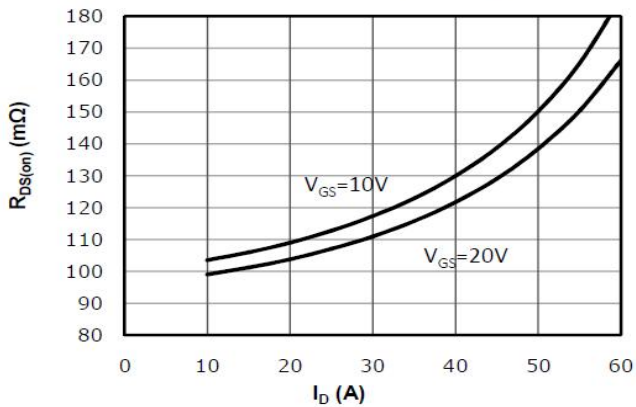


Fig 6: $R_{DS(on)}$ vs. Temperature

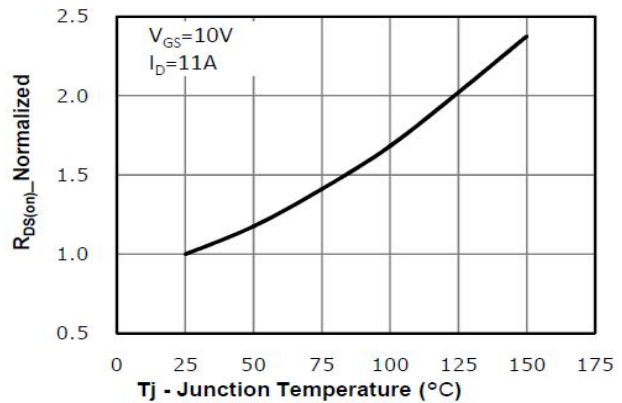


Fig 7: BVDSS vs. Temperature

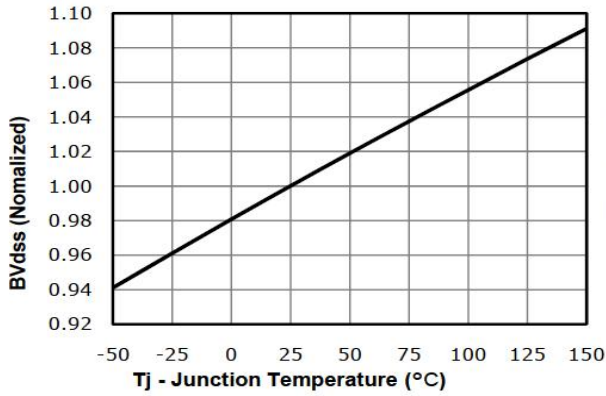


Fig 8: Rds(on) vs Gate Voltage

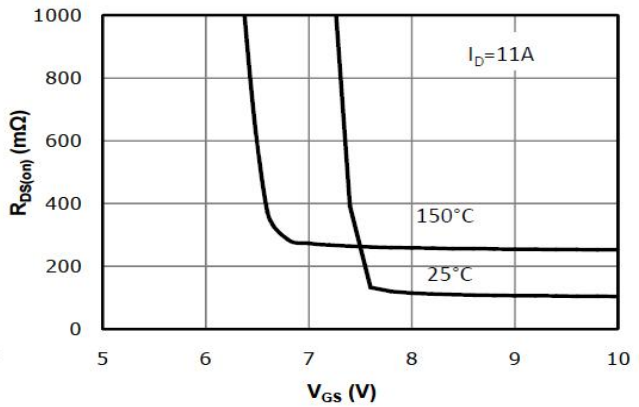


Fig 9: Body-diode Forward Characteristics

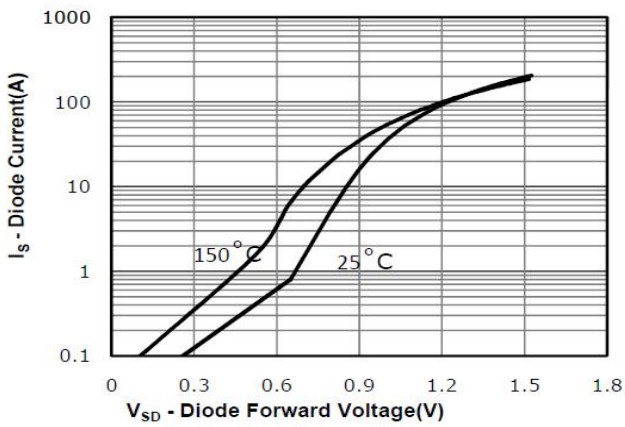


Fig 10: Gate Charge Characteristics

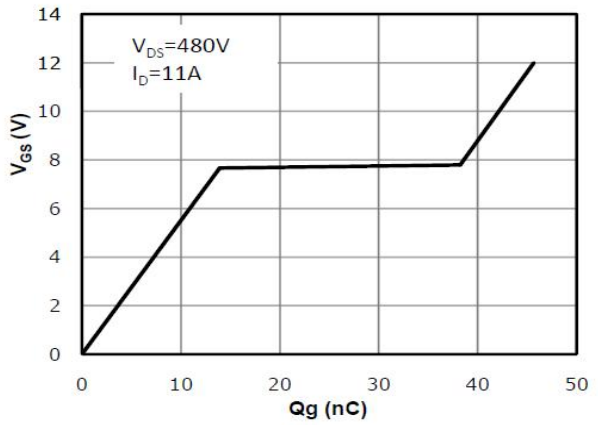


Fig 11: Capacitance Characteristics

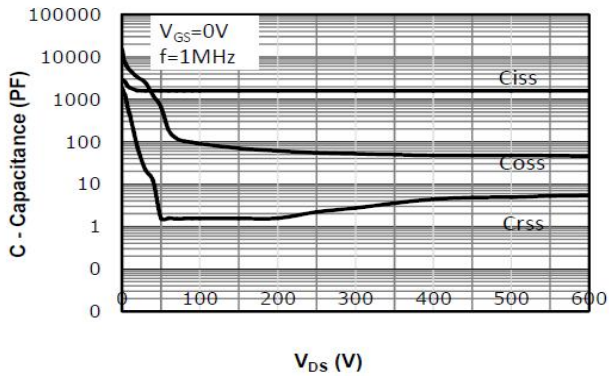


Fig 12: Safe Operating Area

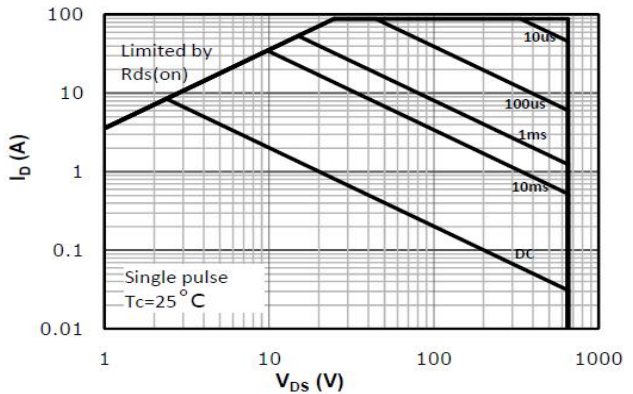
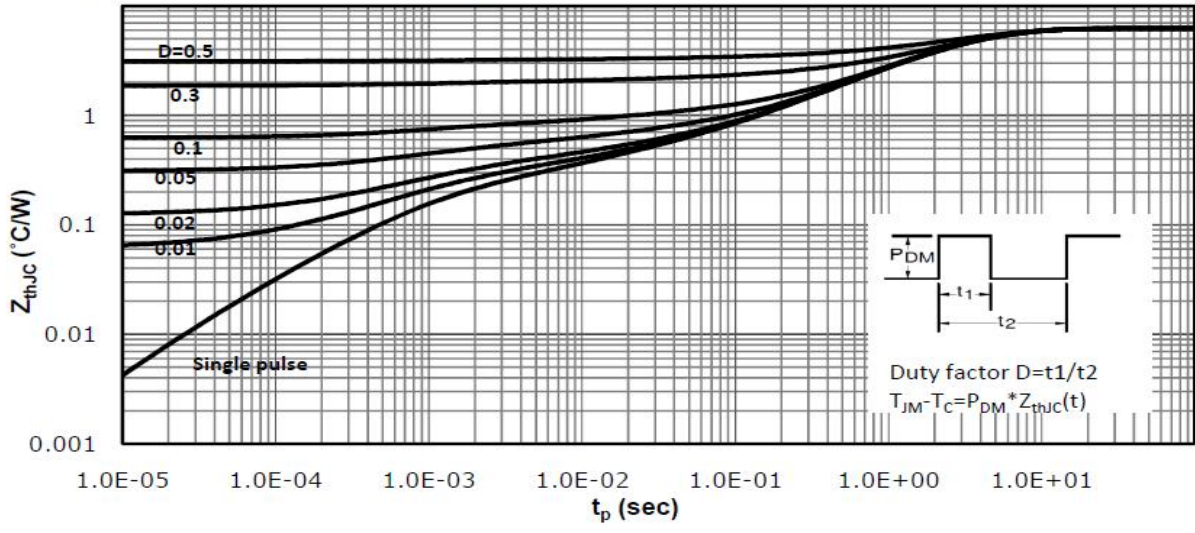
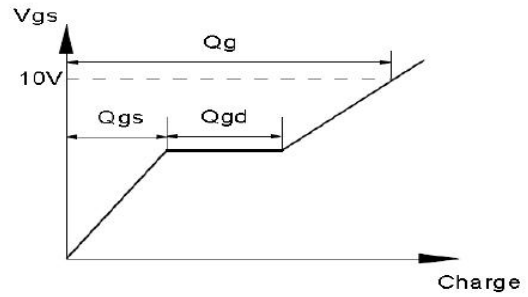
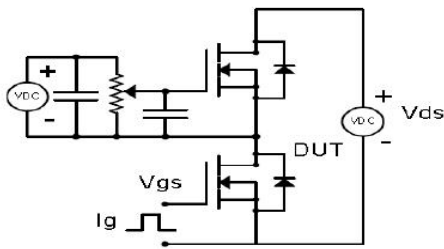


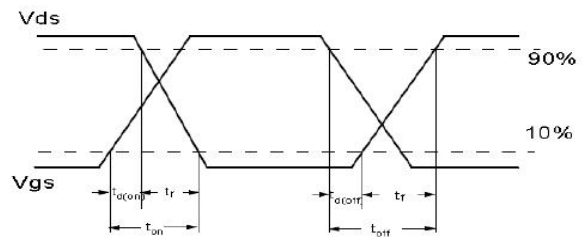
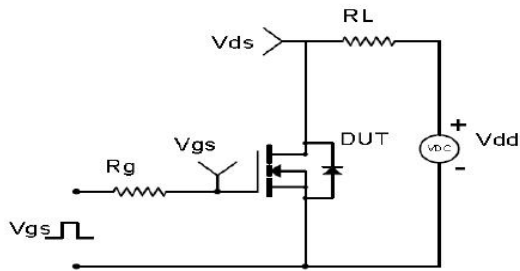
Fig 13: Max. Transient Thermal Impedance



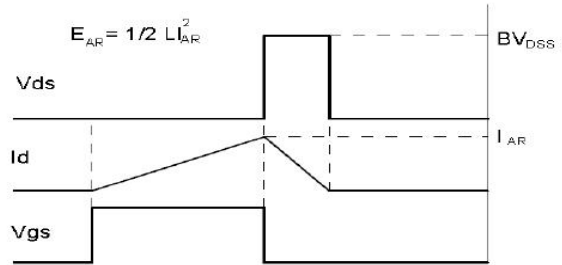
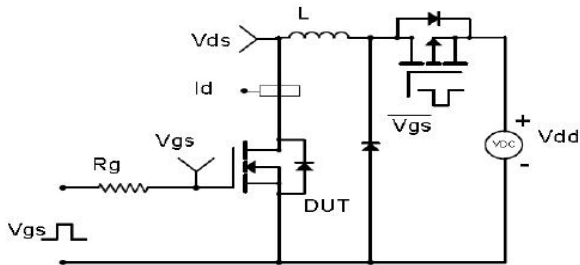
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

