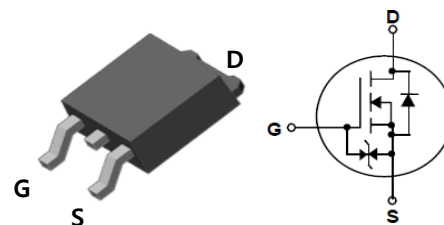


N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: $V_{DS}=850V$ (@ $T_J=150^{\circ}C$)
- Low drain-source On resistance: $R_{DS(on)}=0.85\Omega$ (Max.)
- Built-in ESD Diode
- RoHS compliant and Halogen free device
- 100% avalanche tested

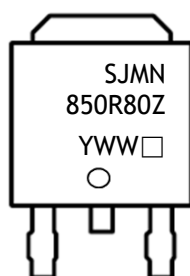


TO-252

Ordering Information

Part Number	Marking	Package
SJMN850R80ZD	SJMN850R80Z	TO-252

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW□
 -. YWW: Date Code (year, week)
 -. □: Factory Management Code

Absolute maximum ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	800	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current (DC) (Note 1)	I_D	$T_C=25^{\circ}C$	6.6
		$T_C=100^{\circ}C$	4.2
Drain current (Pulsed) (Note 1)	I_{DM}	19.8	A
Single pulsed avalanche energy (Note 2)	E_{AS}	90	mJ
Single avalanche current (Note 2)	I_{AS}	1.4	A
Diode dv/dt ruggedness (Note 3)	dv/dt	15	V/ns
MOSFET dv/dt ruggedness (Note 4)	dv/dt	50	V/ns
Power dissipation	P_D	66	W
Gate to source ESD (Human Body Model)	$V_{ESD(G-S)}$	2000	V
Junction temperature	T_J	150	$^{\circ}C$
Storage temperature range	T_{stg}	-55~150	$^{\circ}C$

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.89	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=1\text{mA}$, $V_{GS}=0$	800	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=220\mu\text{A}$, $V_{DS}=V_{GS}$	2	-	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=800\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=800\text{V}$, $T_C=150^\circ\text{C}$	-	-	100	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 1	μA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=1.6\text{A}$	-	0.71	0.85	Ω
Input capacitance	C_{iss}	$V_{DS}=200\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	605	-	pF
Output capacitance	C_{oss}		-	16	-	
Reverse transfer capacitance	C_{rss}		-	1	-	
Turn-on delay time (Note 5)	$t_{d(on)}$	$V_{DD}=400\text{V}$, $I_D=2.8\text{A}$, $R_G=25\Omega$	-	40	-	ns
Rise time (Note 5)	t_r		-	48	-	
Turn-off delay time (Note 5)	$t_{d(off)}$		-	68	-	
Fall time (Note 5)	t_f		-	45	-	
Total gate charge (Note 6)	Q_g	$V_{DS}=640\text{V}$, $V_{GS}=10\text{V}$, $I_D=2.8\text{A}$	-	15	-	nC
Gate-source charge (Note 6)	Q_{gs}		-	6	-	
Gate-drain charge (Note 6)	Q_{gd}		-	2	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	6.6	A
Source current (Pulsed)	I_{SM}		-	-	19.8	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=2.8\text{A}$	-	-	1.3	V
Reverse recovery time (Note 5,6)	t_{rr}	$I_S=2.8\text{A}$, $V_{GS}=0\text{V}$ $dI_F/dt=-100\text{A}/\mu\text{s}$	-	289	-	ns
Reverse recovery charge (Note 5,6)	Q_{rr}		-	1.7	-	μC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. $L=86\text{mH}$, $I_{AS}=1.4\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. $I_S \leq 6.6\text{A}$, $V_{DS} \leq 400\text{V}$, $dI_S/dt \leq 100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$
4. $V_{DS} \leq 400\text{V}$, $I_S \leq 6.6\text{A}$
5. Guaranteed by design, not subject to production testing
6. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

Typical Characteristics Curve

Fig. 1 $I_D - V_{DS}$

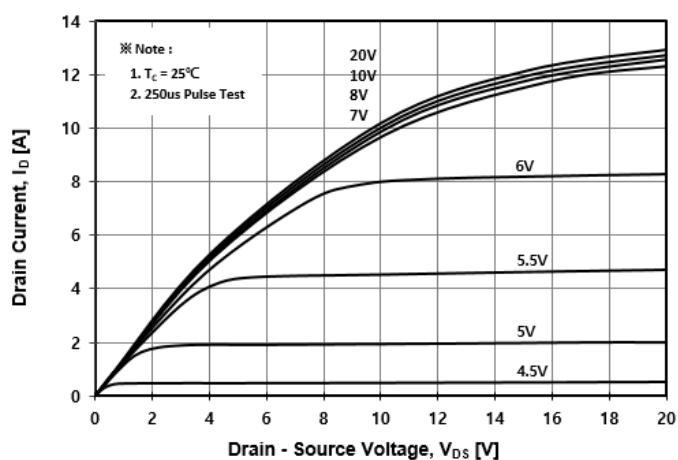


Fig. 2 $I_D - V_{GS}$

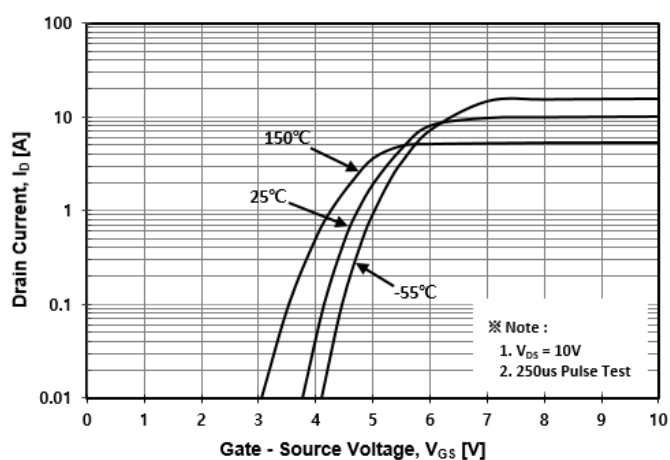


Fig. 3 $R_{DS(ON)} - I_D$

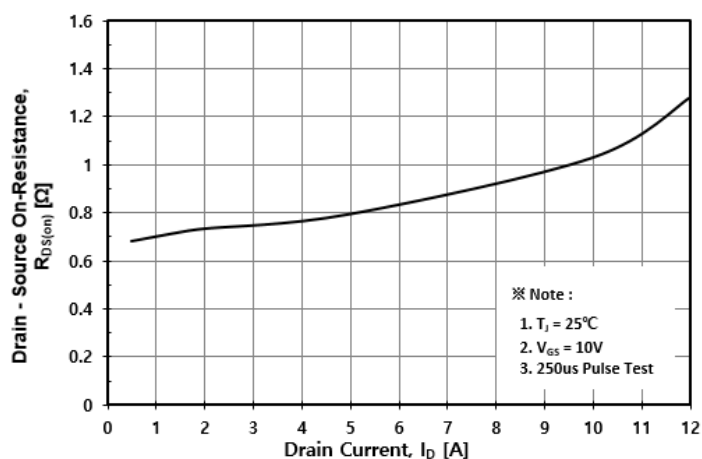


Fig. 4 $I_S - V_{SD}$

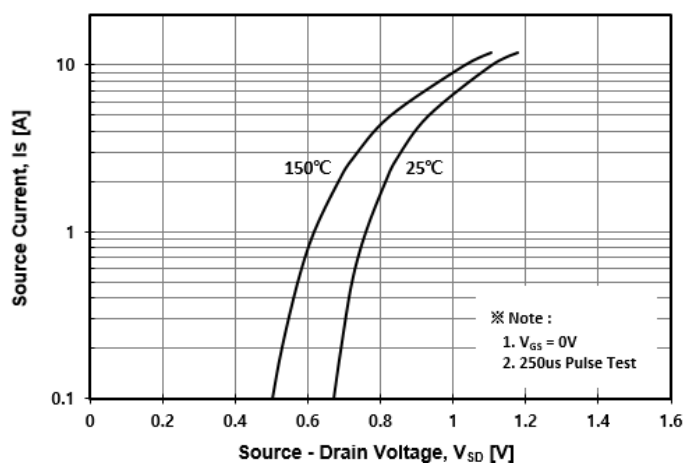


Fig. 5 Capacitance - V_{DS}

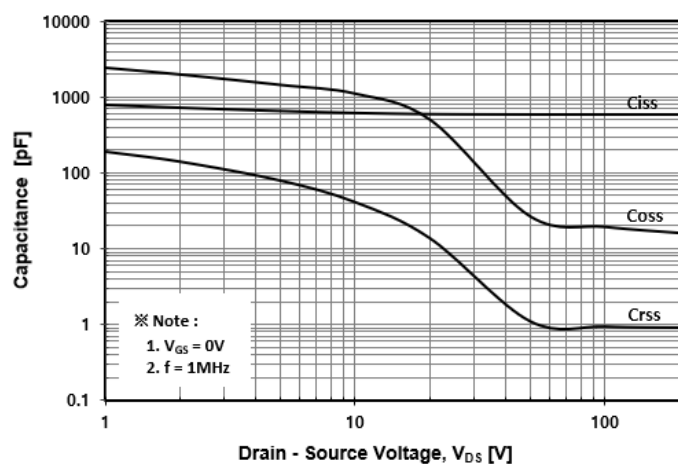
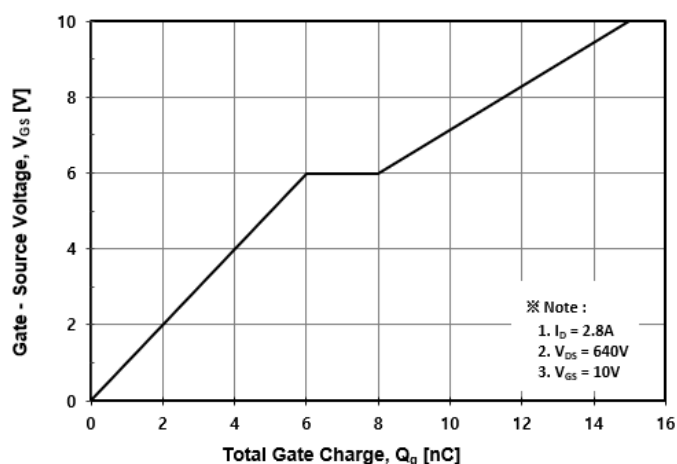


Fig. 6 $V_{GS} - Q_G$



Typical Characteristics Curve (Continue)

Fig. 7 $BV_{DSS} - T_J$

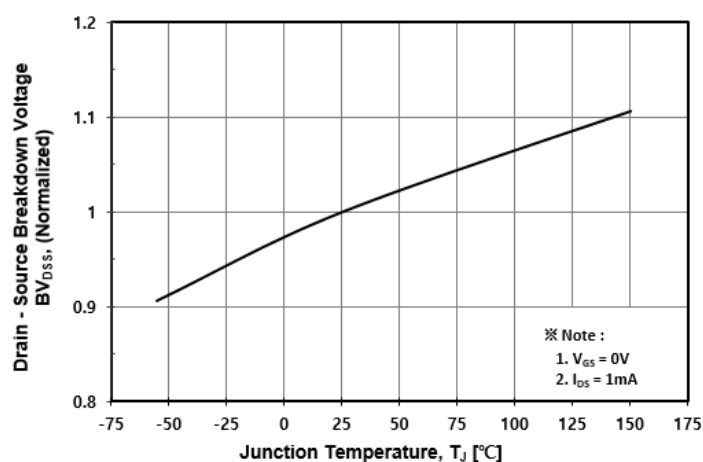


Fig. 8 $R_{DS(ON)} - T_J$

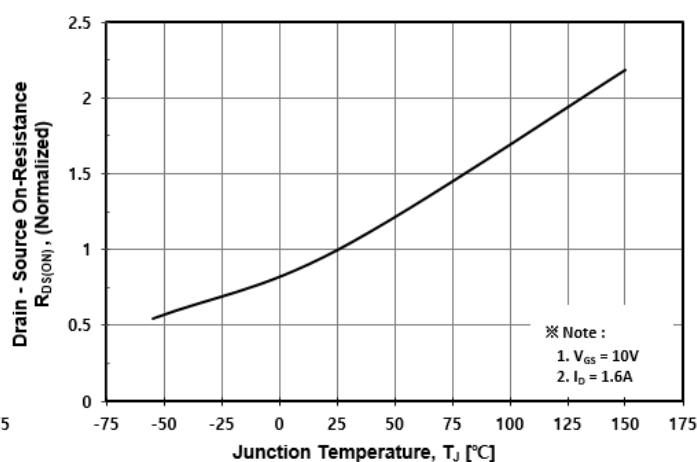


Fig. 9 $I_D - T_C$

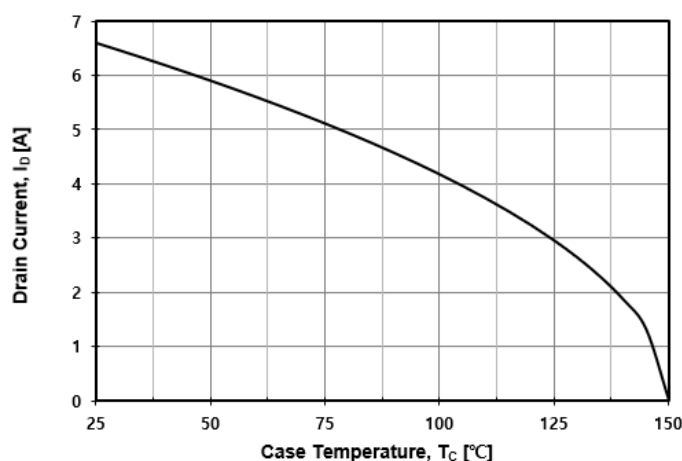


Fig. 10 Safe Operating Area

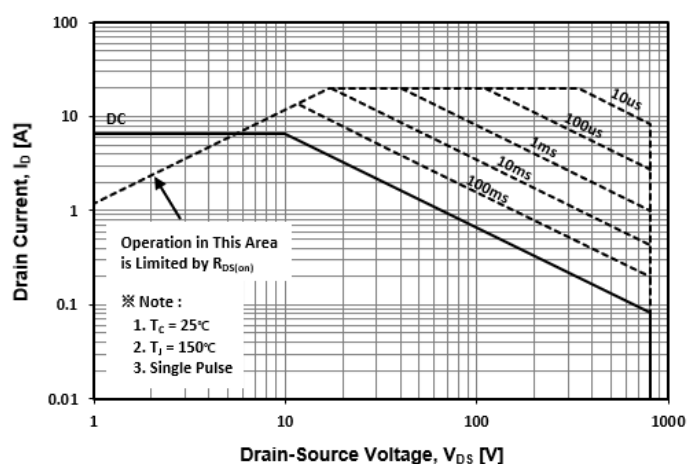


Fig. 11 Transient Thermal Impedance

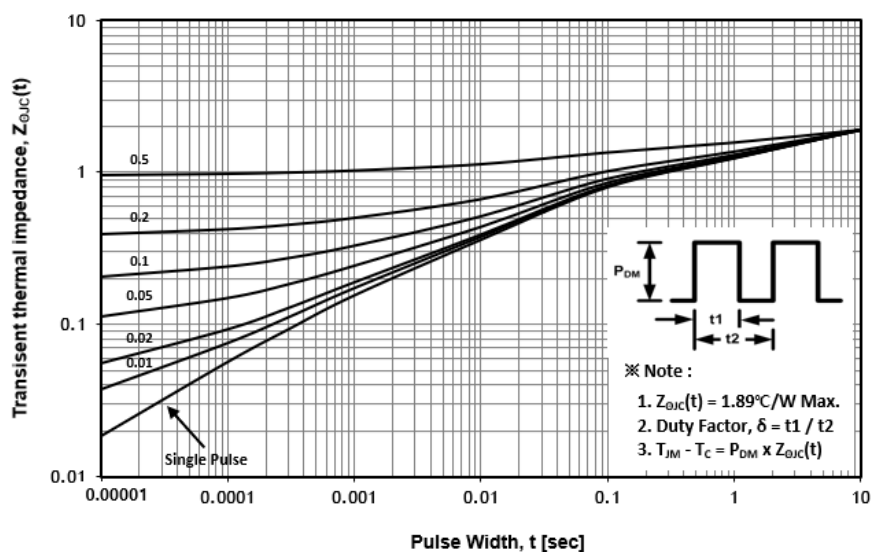


Fig. 12 Gate Charge Test Circuit & Waveform

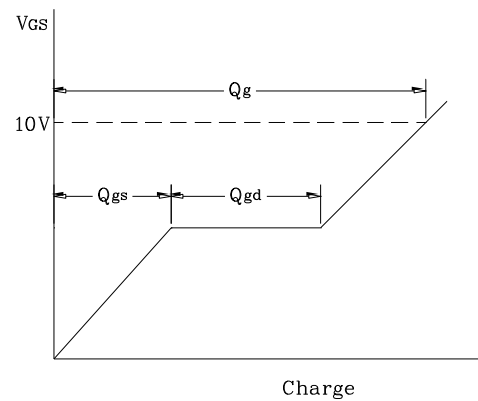
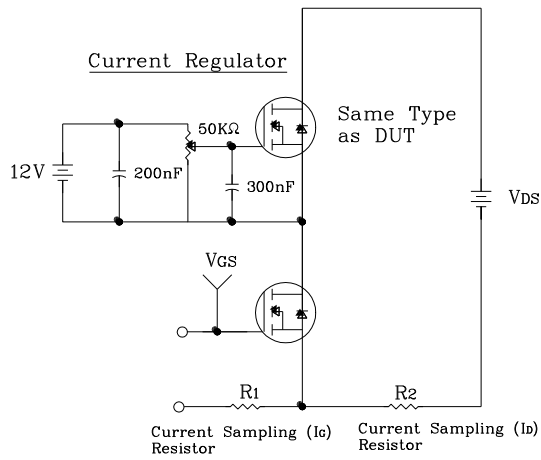


Fig. 13 Resistive Switching Test Circuit & Waveform

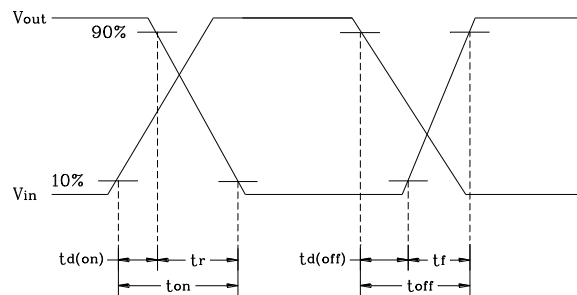
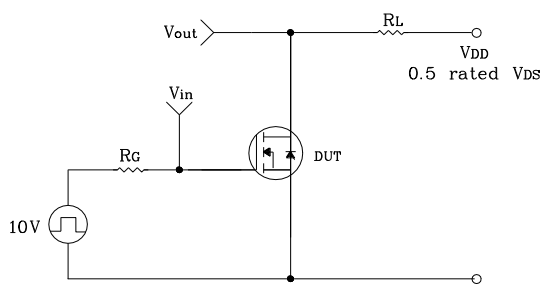


Fig. 14 E_{AS} Test Circuit & Waveform

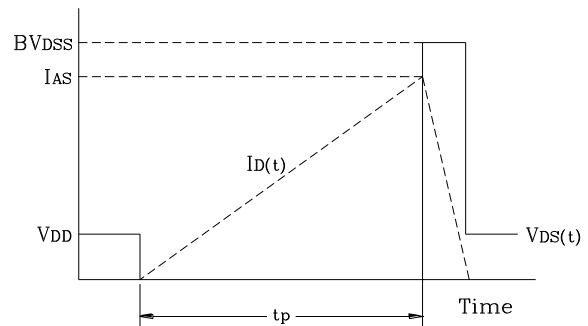
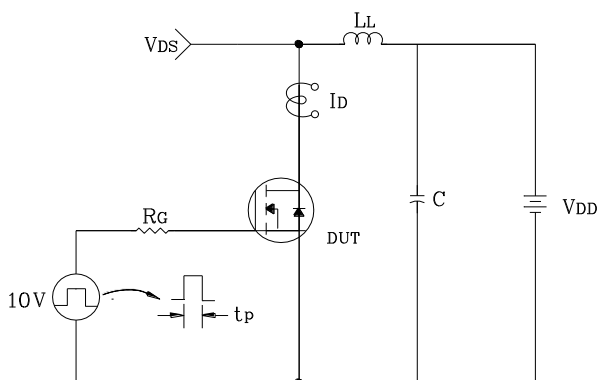
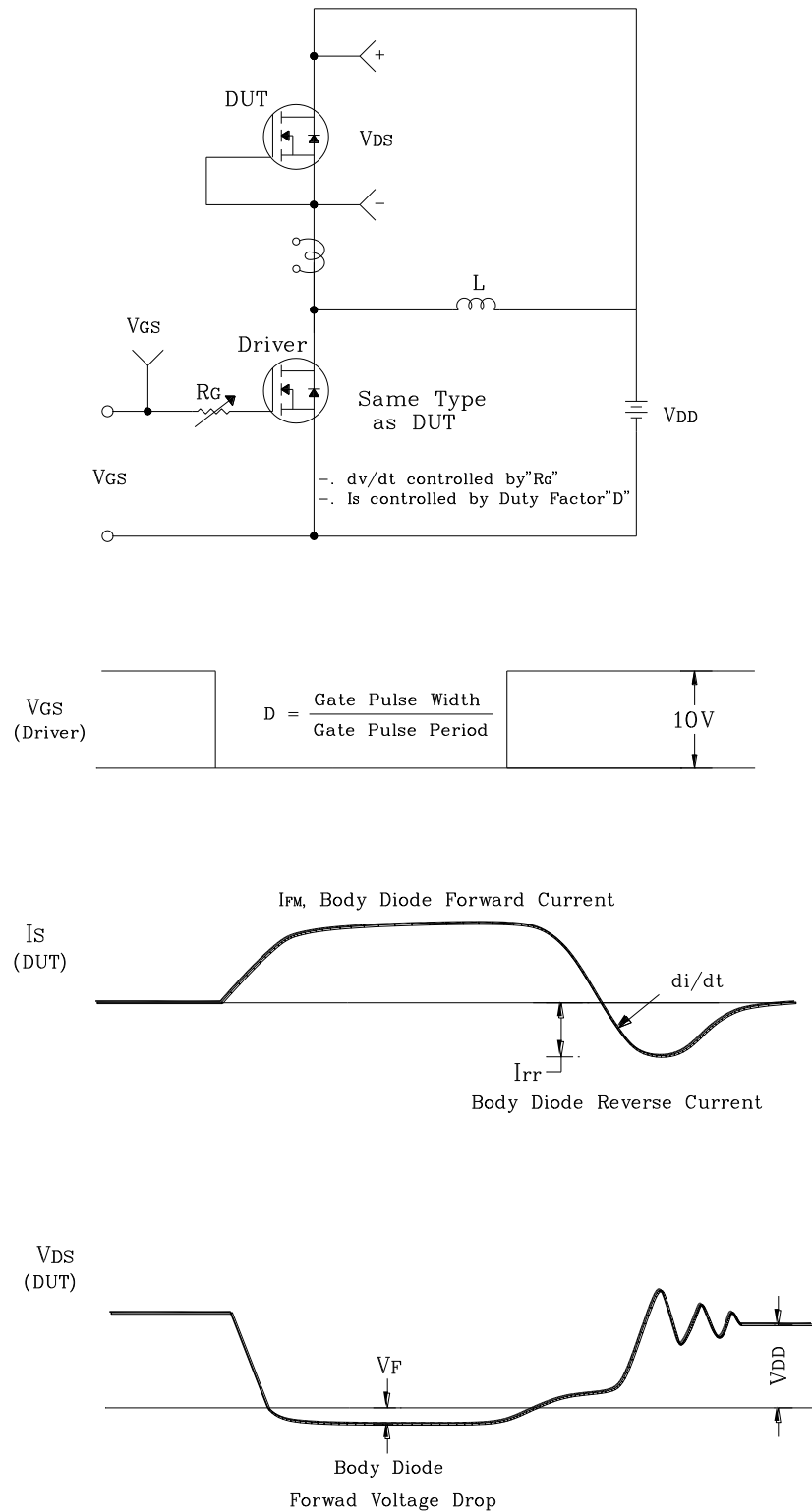
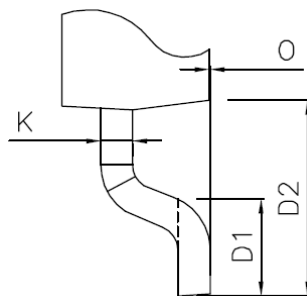
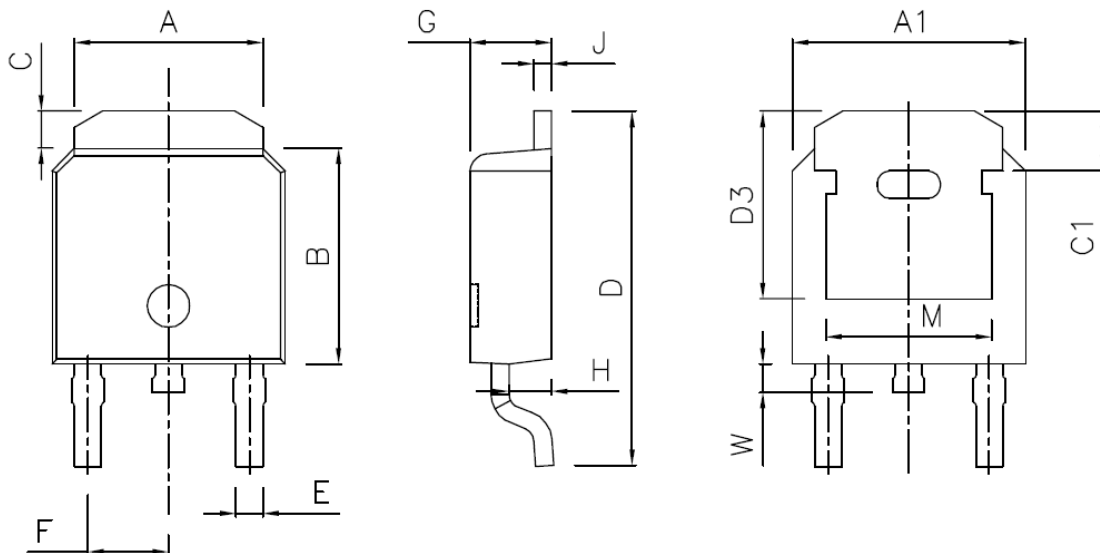


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS		
	MIN	NOR	MAX
A	5.03	5.34	5.64
A1	6.30	6.60	6.90
B	5.70	6.00	6.30
C	0.75	1.05	1.35
C1	1.021	1.321	1.621
D	9.65	9.95	10.25
D1	1.30	1.50	1.70
D2	2.70	2.90	3.10
D3	5.00	5.30	5.60
E	0.61	0.76	0.91
F	2.13	2.28	2.43
G	2.00	2.30	2.60
H	0.76	1.06	1.36
J	0.36	0.51	0.66
K	0.37	0.52	0.67
M	4.55	4.85	5.15
O	0.00	0.07	0.17
W	0.60	0.90	1.20

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