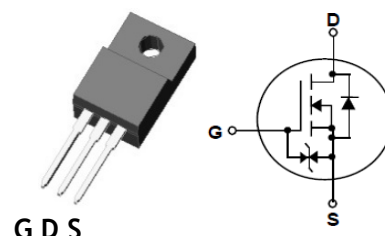


## 800V N-Channel Super Junction MOSFET

### Features

- Very Low FOM ( $R_{DS(on)} \times Q_g$ )
- Extremely low switching loss
- Excellent stability and uniformity
- 100% avalanche tested
- Built-in ESD Diode

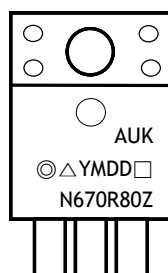


TO-220F-3L

### Ordering Information

| Part Number  | Marking  | Package    |
|--------------|----------|------------|
| SJMN670R80ZF | N670R80Z | TO-220F-3L |

### Marking Information



Column 1: Manufacturer Logo  
Column 2: Production Information  
-  $\odot$ : Management Code  
-  $\triangle$ : Machine Code  
- YMDD: Date Code Marking (Year, Month, Day)  
-  $\square$ : Factory Management Code  
Column 3: Device Code

### Absolute maximum ratings ( $T_c=25^\circ\text{C}$ unless otherwise noted)

| Characteristic                          | Symbol         | Rating                  | Unit             |
|-----------------------------------------|----------------|-------------------------|------------------|
| Drain-source voltage                    | $V_{DS}$       | 800                     | V                |
| Gate-source voltage                     | $V_{GS}$       | $\pm 20$                | V                |
| Drain current (DC) (Note 1)             | $I_D$          | $T_c=25^\circ\text{C}$  | 8                |
|                                         |                | $T_c=100^\circ\text{C}$ | 5.1              |
| Drain current (Pulsed) (Note 1)         | $I_{DM}$       | 24                      | A                |
| Single pulsed avalanche energy (Note 2) | $E_{AS}$       | 96                      | mJ               |
| Single avalanche current (Note 2)       | $I_{AS}$       | 1.45                    | A                |
| Diode dv/dt ruggedness (Note 3)         | dv/dt          | 15                      | V/ns             |
| MOSFET dv/dt ruggedness (Note 4)        | dv/dt          | 50                      | V/ns             |
| Power dissipation                       | $P_D$          | 29                      | W                |
| Gate to source ESD (Human Body Model)   | $V_{ESD(G-S)}$ | 2000                    | V                |
| Junction temperature                    | $T_J$          | 150                     | $^\circ\text{C}$ |
| Storage temperature range               | $T_{stg}$      | -55~150                 | $^\circ\text{C}$ |

## Thermal Characteristics

| Characteristic                          | Symbol        | Rating    | Unit |
|-----------------------------------------|---------------|-----------|------|
| Thermal resistance, junction to case    | $R_{th(j-c)}$ | Max. 4.31 | °C/W |
| Thermal resistance, junction to ambient | $R_{th(j-a)}$ | Max. 62.5 |      |

Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)

| Characteristic                 | Symbol       | Test Condition                                                    | Min. | Typ. | Max.    | Unit          |
|--------------------------------|--------------|-------------------------------------------------------------------|------|------|---------|---------------|
| Drain-source breakdown voltage | $BV_{DSS}$   | $I_D=1\text{mA}$ , $V_{GS}=0$                                     | 800  | -    | -       | V             |
| Gate threshold voltage         | $V_{GS(th)}$ | $I_D=280\mu\text{A}$ , $V_{DS}=V_{GS}$                            | 2    | -    | 4       | V             |
| Drain-source cut-off current   | $I_{DSS}$    | $V_{DS}=800\text{V}$ , $V_{GS}=0\text{V}$                         | -    | -    | 1       | $\mu\text{A}$ |
|                                |              | $V_{DS}=800\text{V}$ , $T_C=150^{\circ}\text{C}$                  | -    | -    | 100     | $\mu\text{A}$ |
| Gate leakage current           | $I_{GSS}$    | $V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$                      | -    | -    | $\pm 1$ | $\mu\text{A}$ |
| Drain-source on-resistance     | $R_{DS(ON)}$ | $V_{GS}=10\text{V}$ , $I_D=2\text{A}$                             | -    | 0.58 | 0.67    | $\Omega$      |
| Input capacitance              | $C_{iss}$    | $V_{DS}=200\text{V}$ , $V_{GS}=0\text{V}$ ,<br>$f=1.0\text{MHz}$  | -    | 716  | -       | pF            |
| Output capacitance             | $C_{oss}$    |                                                                   | -    | 17.2 | -       |               |
| Reverse transfer capacitance   | $C_{rss}$    |                                                                   | -    | 1.0  | -       |               |
| Turn-on delay time (Note 5)    | $t_{d(on)}$  | $V_{DD}=400\text{V}$ , $I_D=3.6\text{A}$ ,<br>$R_G=25\Omega$      | -    | 40   | -       | ns            |
| Rise time (Note 5)             | $t_r$        |                                                                   | -    | 46   | -       |               |
| Turn-off delay time (Note 5)   | $t_{d(off)}$ |                                                                   | -    | 79   | -       |               |
| Fall time (Note 5)             | $t_f$        |                                                                   | -    | 45   | -       |               |
| Total gate charge (Note 6)     | $Q_g$        | $V_{DS}=640\text{V}$ , $V_{GS}=10\text{V}$ ,<br>$I_D=3.6\text{A}$ | -    | 25   | -       | nC            |
| Gate-source charge (Note 6)    | $Q_{gs}$     |                                                                   | -    | 8    | -       |               |
| Gate-drain charge (Note 6)     | $Q_{gd}$     |                                                                   | -    | 9    | -       |               |

Source-Drain Diode Ratings and Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)

| Characteristic                     | Symbol   | Test Condition                                                               | Min. | Typ. | Max. | Unit          |
|------------------------------------|----------|------------------------------------------------------------------------------|------|------|------|---------------|
| Source current (DC)                | $I_S$    | Integral reverse diode<br>in the MOSFET                                      | -    | -    | 8    | A             |
| Source current (Pulsed)            | $I_{SM}$ |                                                                              | -    | -    | 24   | A             |
| Forward voltage                    | $V_{SD}$ | $V_{GS}=0\text{V}$ , $I_S=3.6\text{A}$                                       | -    | -    | 1.3  | V             |
| Reverse recovery time (Note 5,6)   | $t_{rr}$ | $I_S=3.6\text{A}$ , $V_{GS}=0\text{V}$<br>$dI_F/dt=-100\text{A}/\mu\text{s}$ | -    | 304  | -    | ns            |
| Reverse recovery charge (Note 5,6) | $Q_{rr}$ |                                                                              | -    | 2.4  | -    | $\mu\text{C}$ |

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2.  $I_{AS}=1.45\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^{\circ}\text{C}$
3.  $I_S \leq 8\text{A}$ ,  $V_{DS} \leq 400\text{V}$ ,  $dI_S/dt \leq 100\text{A}/\mu\text{s}$ ,  $T_J=25^{\circ}\text{C}$
4.  $V_{DS} \leq 400\text{V}$ ,  $I_S \leq 8\text{A}$
5. Guaranteed by design, not subject to production testing
6. Pulse test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$

## Typical Characteristics Curve

Fig. 1  $I_D - V_{DS}$

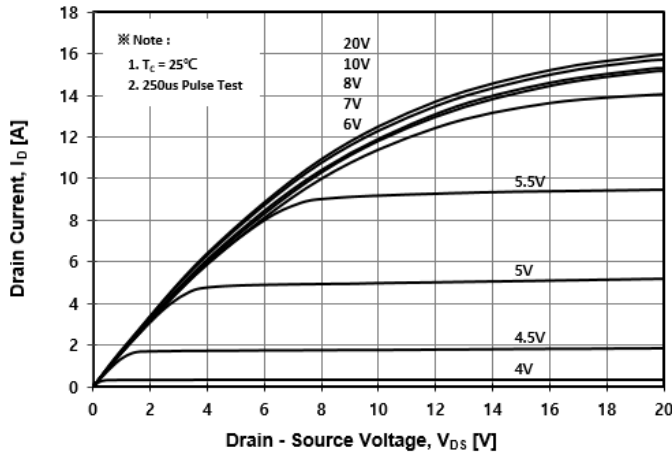


Fig. 2  $I_D - V_{GS}$

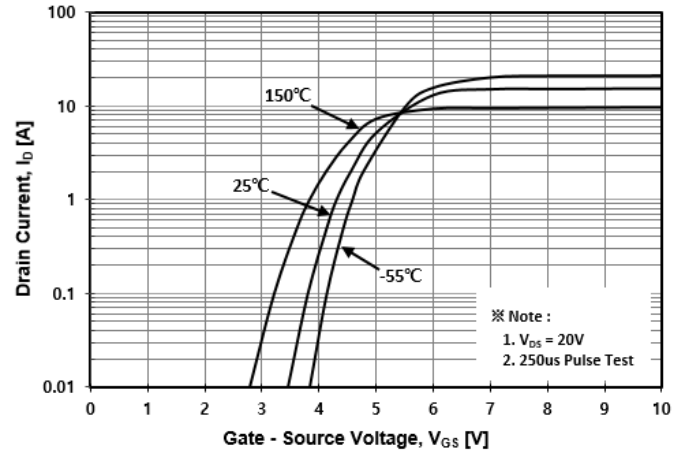


Fig. 3  $R_{DS(ON)} - I_D$

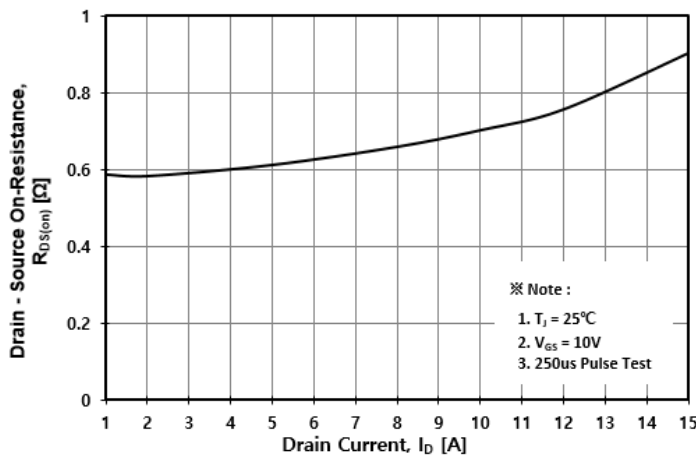


Fig. 4  $I_S - V_{SD}$

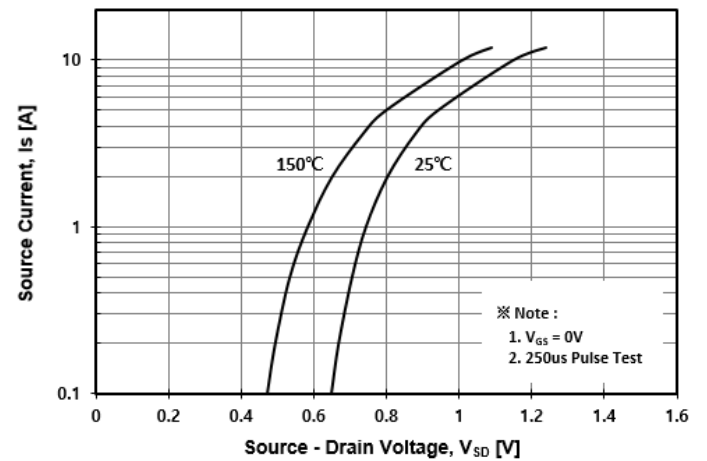


Fig. 5 Capacitance -  $V_{DS}$

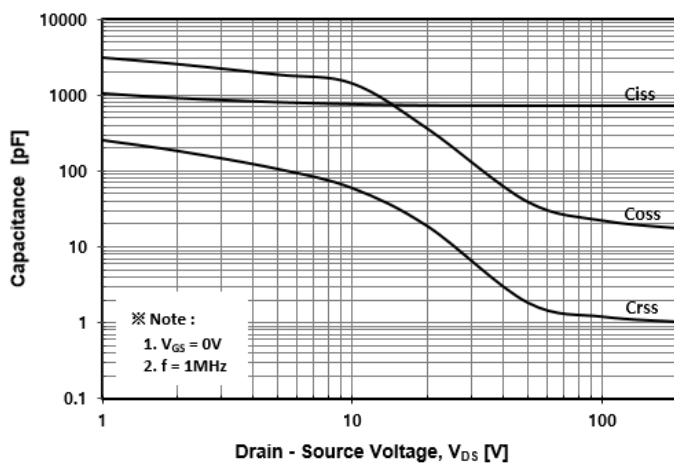
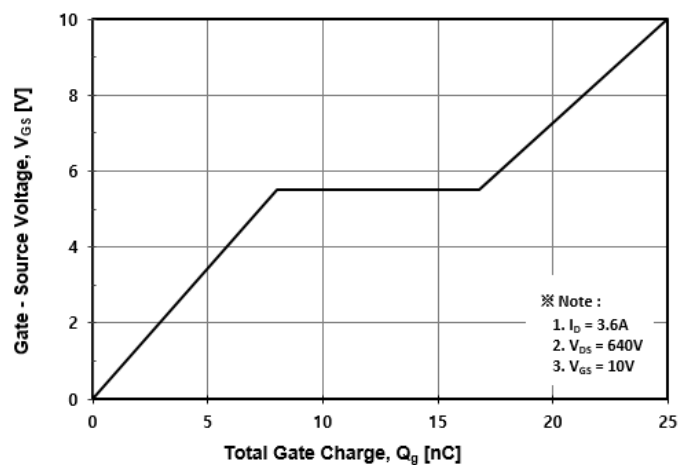


Fig. 6  $V_{GS} - Q_G$



## Typical Characteristics Curve (Continue)

Fig. 7  $BV_{DSS} - T_J$

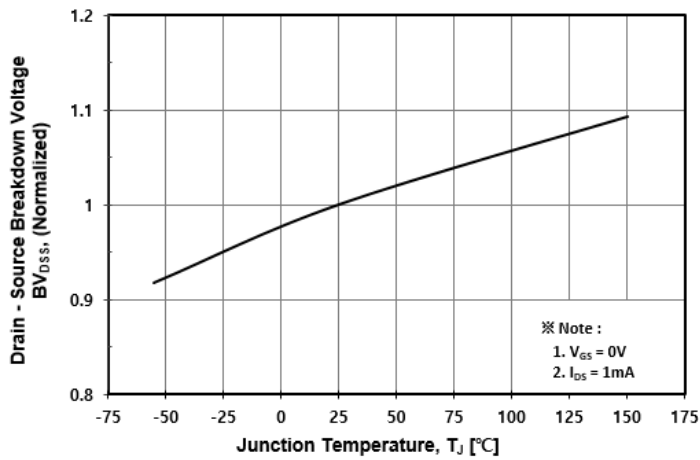


Fig. 8  $R_{DS(ON)} - T_J$

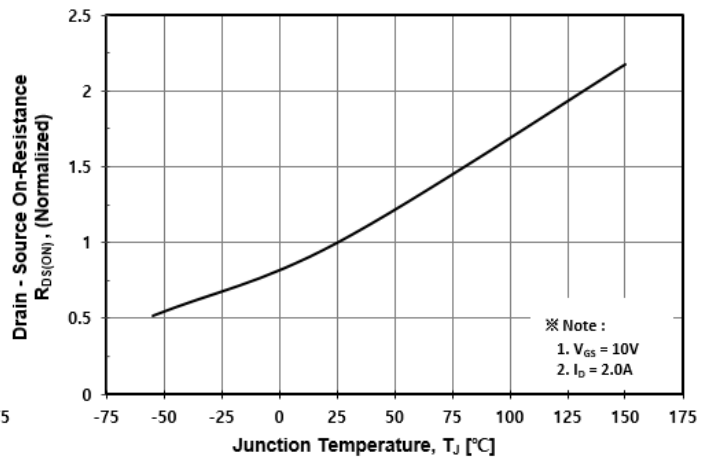


Fig. 9  $I_D - T_C$

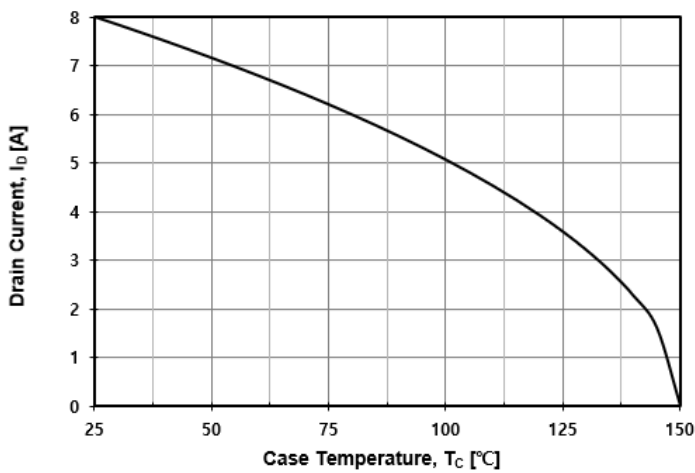


Fig. 10 Safe Operating Area

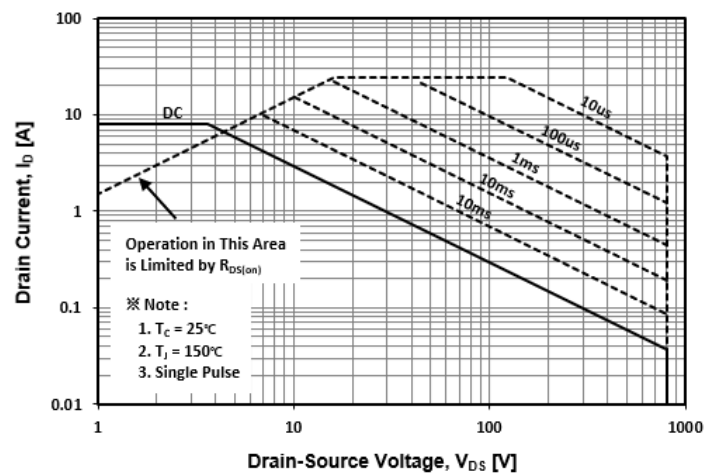


Fig. 11 Transient Thermal Impedance

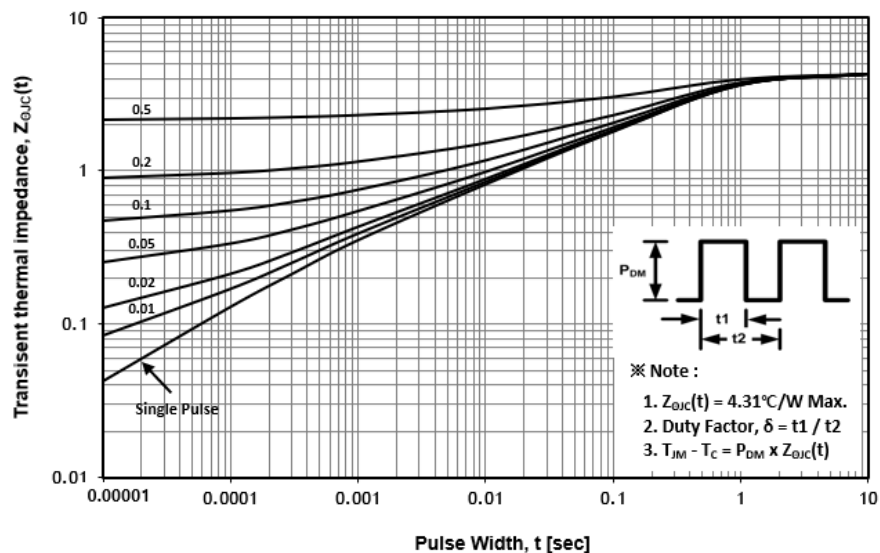


Fig. 12 Gate Charge Test Circuit & Waveform

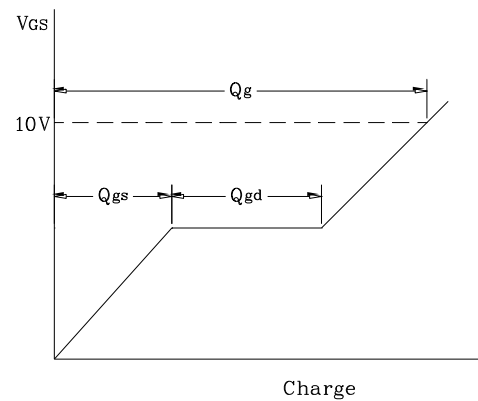
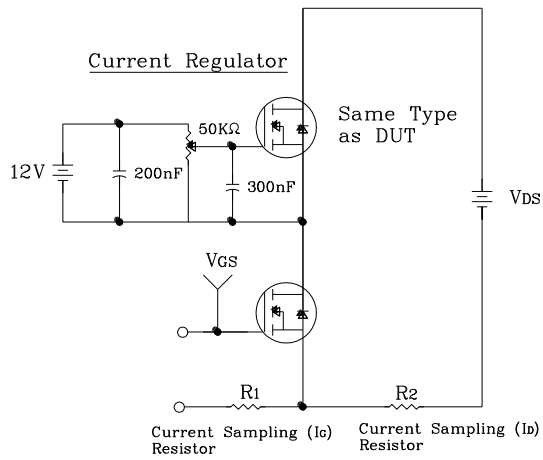


Fig. 13 Resistive Switching Test Circuit & Waveform

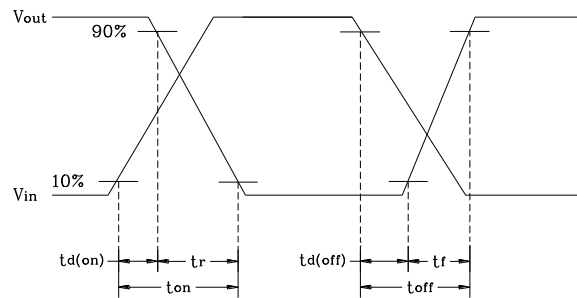
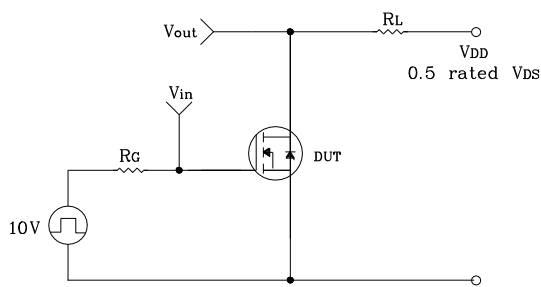
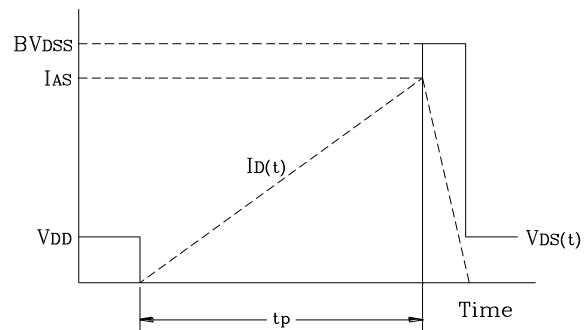
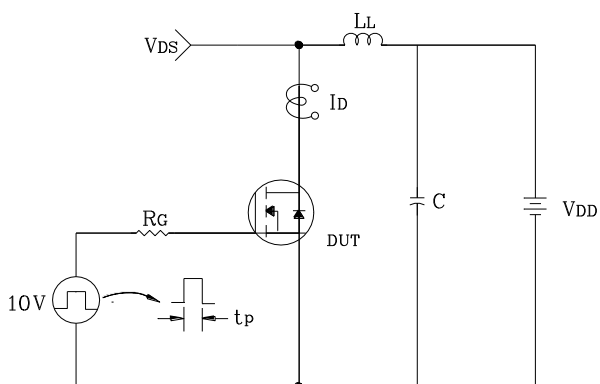
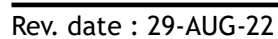
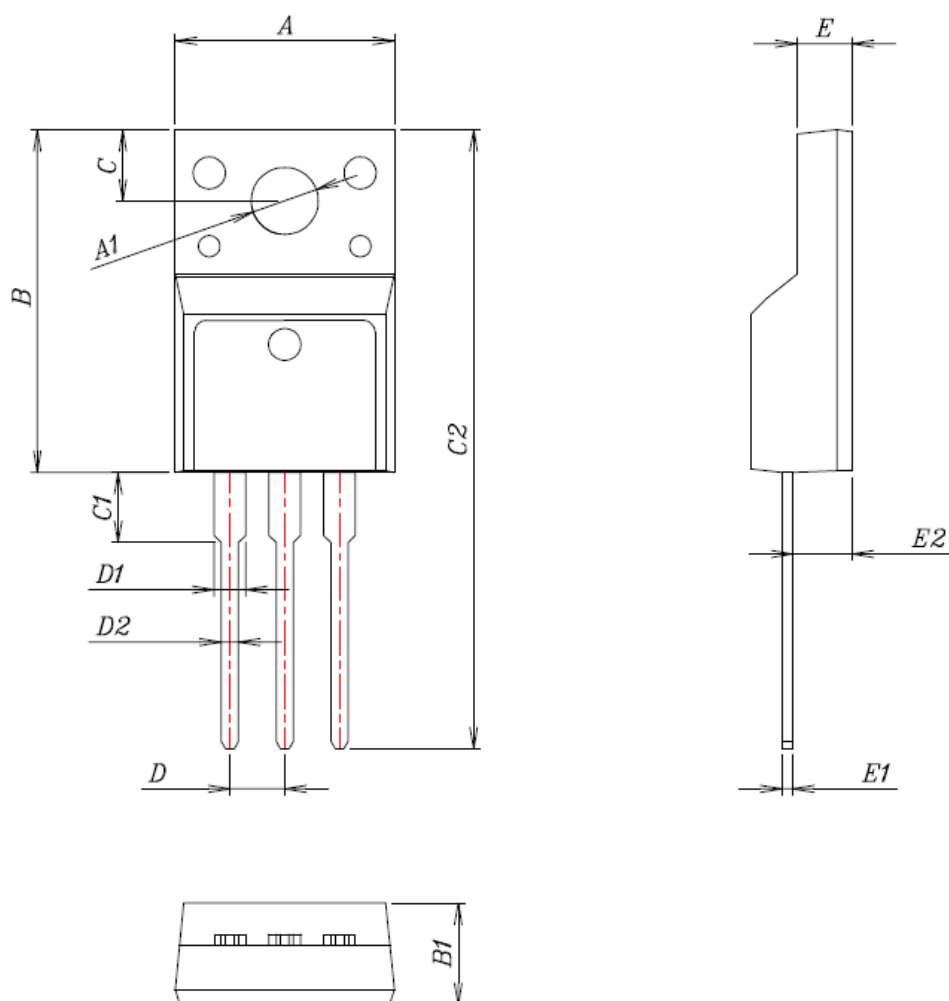


Fig. 14  $E_{AS}$  Test Circuit & Waveform





## Package Outline Dimensions



| SYMBOL | MILLIMETERS  |
|--------|--------------|
| A      | 10.16±0.30   |
| A1     | 3.12±0.20    |
| B      | 15.90±0.50   |
| B1     | 4.70±0.30    |
| C      | 3.30±0.25    |
| C1     | 3.25±0.30    |
| C2     | 28.70±0.50   |
| D      | Typical 2.54 |
| D1     | 1.47(MAX)    |
| D2     | 0.80±0.20    |
| E      | 2.55±0.25    |
| E1     | 0.50±0.20    |
| E2     | 2.75±0.30    |

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