

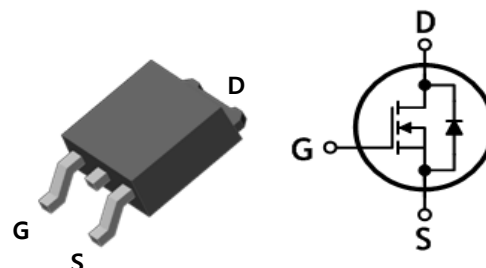
N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: $V_{DS}=700V$ (@ $T_J=150^{\circ}C$)
- Low drain-source On resistance: $R_{DS(on)}=0.6\Omega$ (Max.)
- Ultra low gate charge: $Q_g=12nC$ (Typ.)
- RoHS compliant and Halogen free device
- 100% avalanche tested

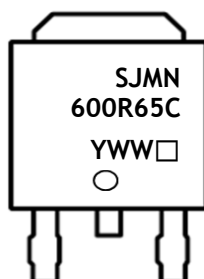
Ordering Information

Part Number	Marking	Package
SJMN600R65CD	SJMN600R65C	TO-252



TO-252

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW□
 -. YWW: Date Code (year, week)
 -. □: Factory Management Code

Absolute maximum ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	650	V
Gate-source voltage	V_{GSS}	± 30	V
Drain current (DC) (Note 1)	I_D	$T_C=25^{\circ}C$	8
		$T_C=100^{\circ}C$	5
Drain current (Pulsed) (Note 1)	I_{DM}	32	A
Single pulsed avalanche energy (Note 2)	E_{AS}	20	mJ
Single avalanche current (Note 2)	I_{AS}	2	A
MOSFET dv/dt ruggedness ($V_{DS} \leq 400V$)	dv/dt	50	V/ns
Diode dv/dt ruggedness ($I_{SD} \leq I_D$, $V_{DS} \leq 400V$)	dv/dt	15	V/ns
Power dissipation	P_D	70	W
Junction temperature	T_J	150	$^{\circ}C$
Storage temperature range	T_{stg}	-55~150	$^{\circ}C$

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.76	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=1\text{mA}$, $V_{GS}=0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=0.5\text{mA}$, $V_{DS}=V_{GS}$	2.5	-	4.5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$	-	-	1	uA
		$V_{DS}=650\text{V}$, $T_J=125^\circ\text{C}$	-	-	100	uA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=4\text{A}$	-	0.51	0.6	Ω
Internal gate resistance	R_g	$f=1\text{MHz}$, Open drain	-	2.6	-	Ω
Input capacitance (Note 3, 4)	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	397	-	pF
Output capacitance (Note 3, 4)	C_{oss}		-	607	-	
Reverse transfer capacitance (Note 3, 4)	C_{rss}		-	24	-	
Turn-on delay time (Note 3, 4)	$t_{d(on)}$	$V_{DS}=350\text{V}$, $I_D=7\text{A}$, $R_G=25\Omega$	-	28	-	ns
Rise time (Note 3, 4)	t_r		-	47	-	
Turn-off delay time (Note 3, 4)	$t_{d(off)}$		-	41	-	
Fall time (Note 3, 4)	t_f		-	47	-	
Total gate charge (Note 3, 4)	Q_g	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=7\text{A}$	-	12	-	nC
Gate-source charge (Note 3, 4)	Q_{gs}		-	6	-	
Gate-drain charge (Note 3, 4)	Q_{gd}		-	2	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	8	A
Source current (Pulsed)	I_{SM}		-	-	32	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=2.5\text{A}$	-	-	1.2	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=7\text{A}$, $V_{GS}=0\text{V}$, $dI_S/dt=100\text{A/us}$	-	239	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	2.2	-	uC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. $L=10\text{mH}$, $V_{DD}=50\text{V}$, Starting $T_J=25^\circ\text{C}$
3. Guaranteed by design, not subject to production testing
4. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

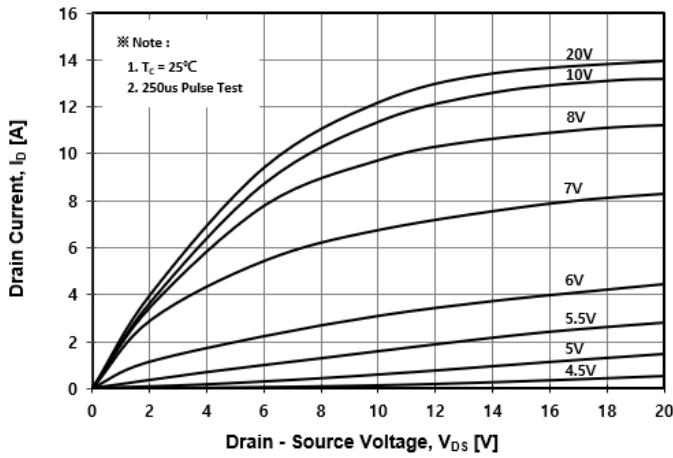


Fig. 2 Typical Transfer Characteristics

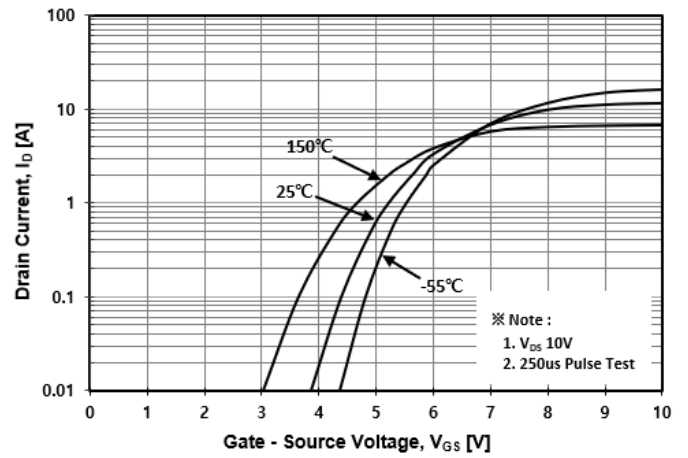


Fig. 3 On-Resistance Variation with Drain Current and Gate Voltage

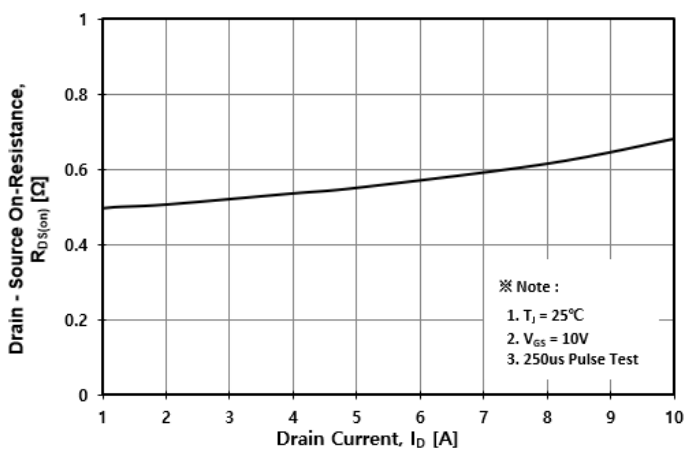


Fig. 4 Body Diode Forward Voltage Variation with Source Current

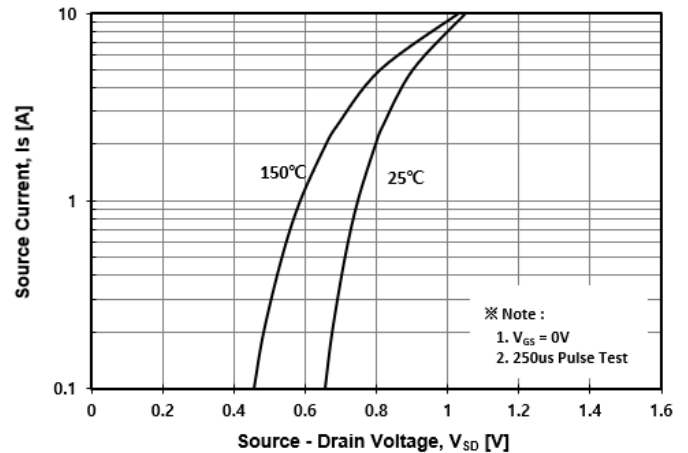


Fig. 5 Typical Capacitance Characteristics

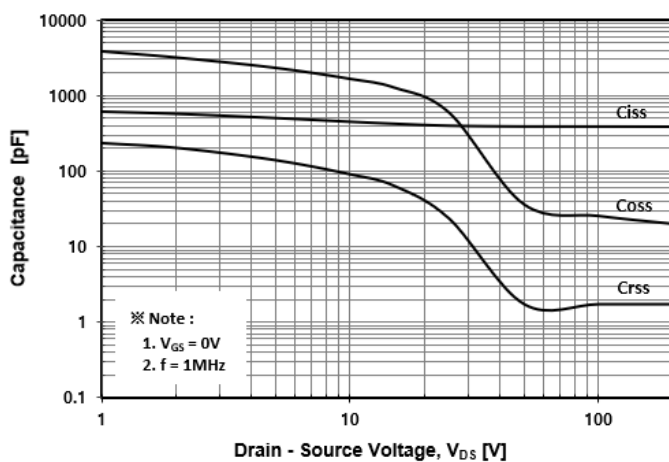
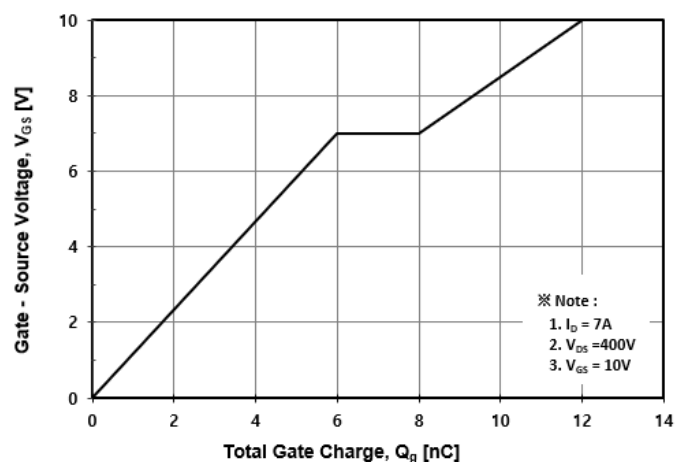


Fig. 6 Typical Total Gate Charge Characteristics



Typical Electrical Characteristics Curves

Fig. 7 Breakdown Voltage Variation vs. Temperature

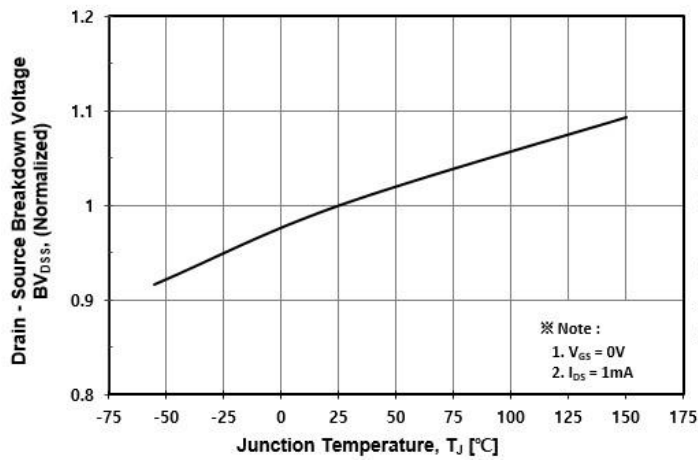


Fig. 8 On-Resistance Variation vs. Temperature

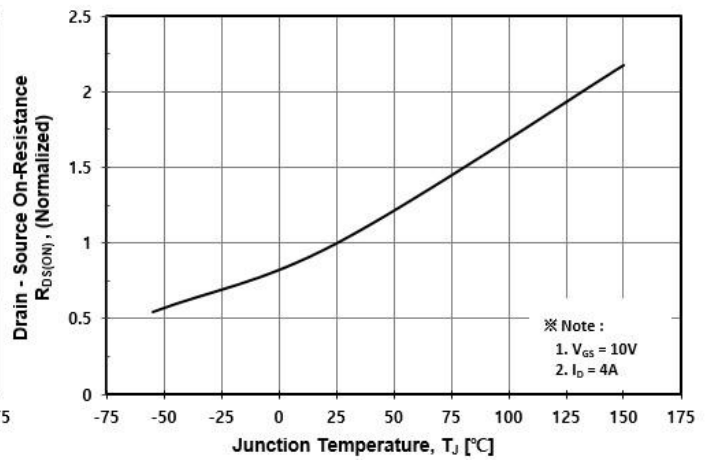


Fig. 9 Maximum Drain Current vs. Case Temperature

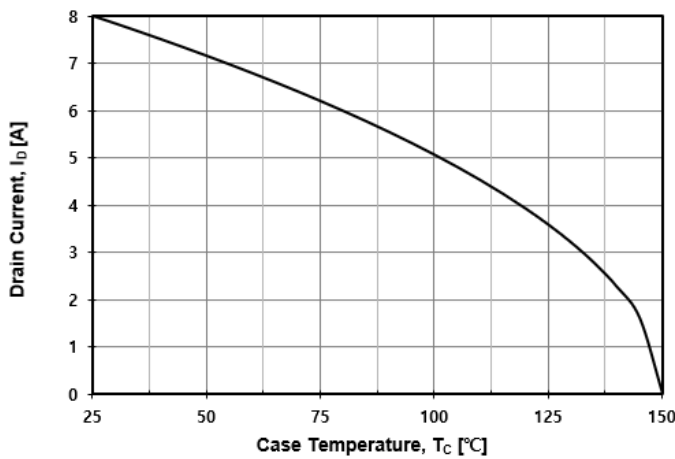


Fig. 10 Maximum Safe Operating Area

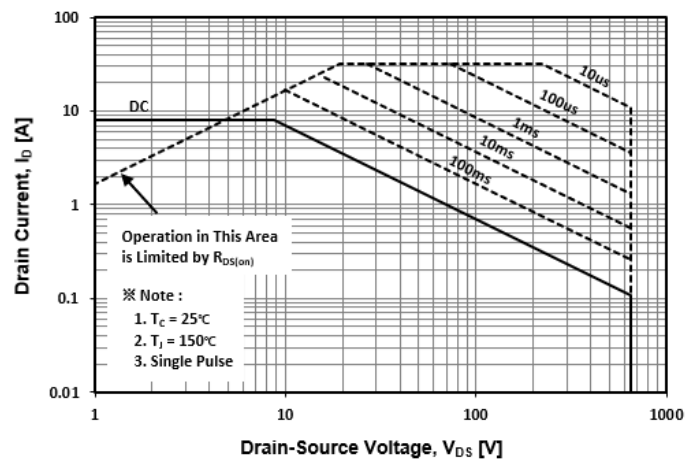


Fig. 11 Transient Thermal Impedance

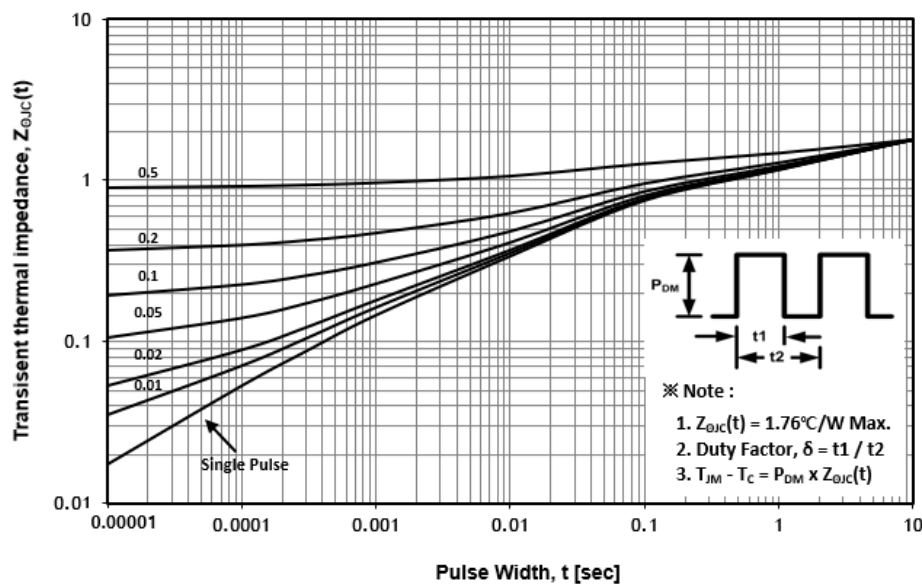


Fig. 12 Gate Charge Test Circuit & Waveform

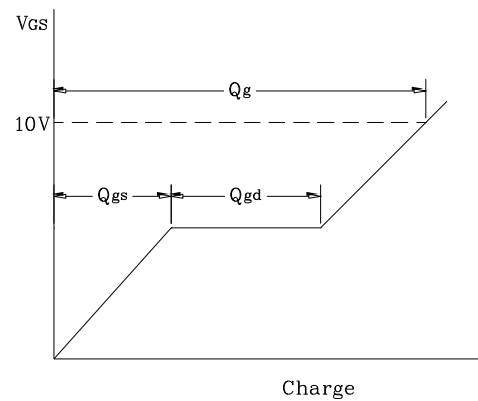
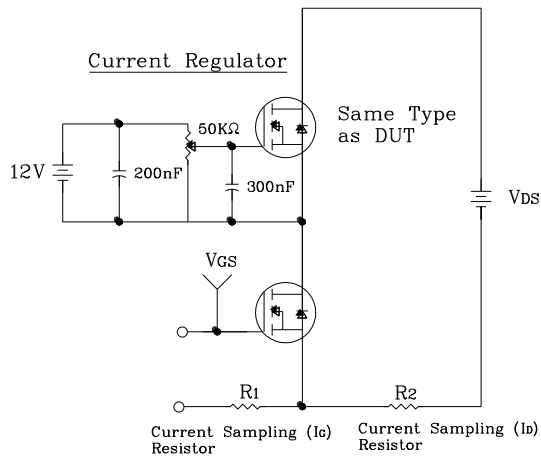


Fig. 13 Resistive Switching Test Circuit & Waveform

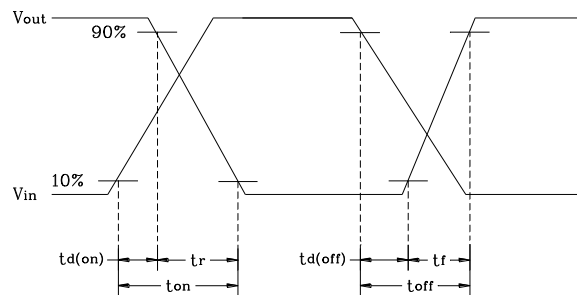
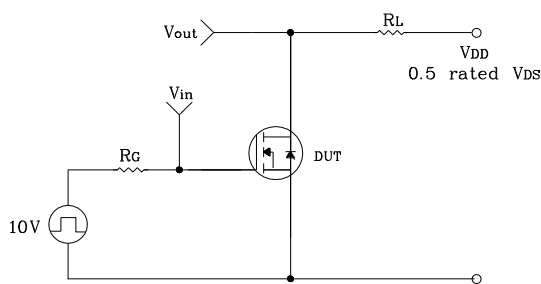


Fig. 14 E_{AS} Test Circuit & Waveform

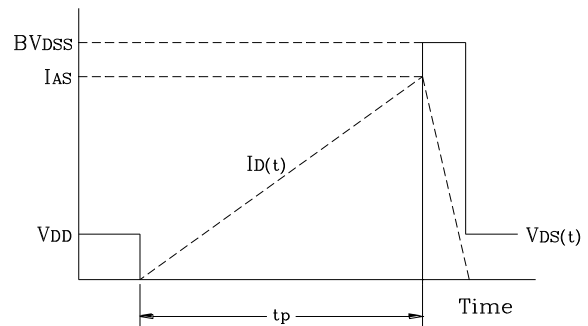
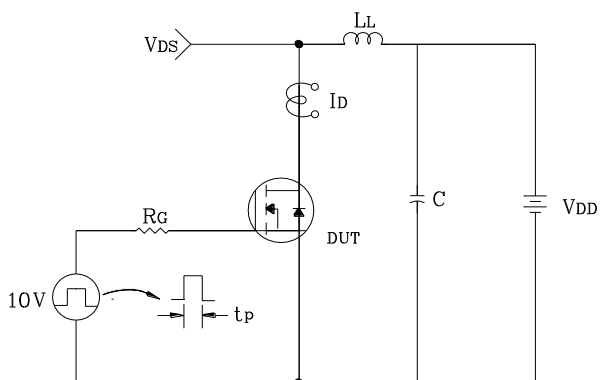
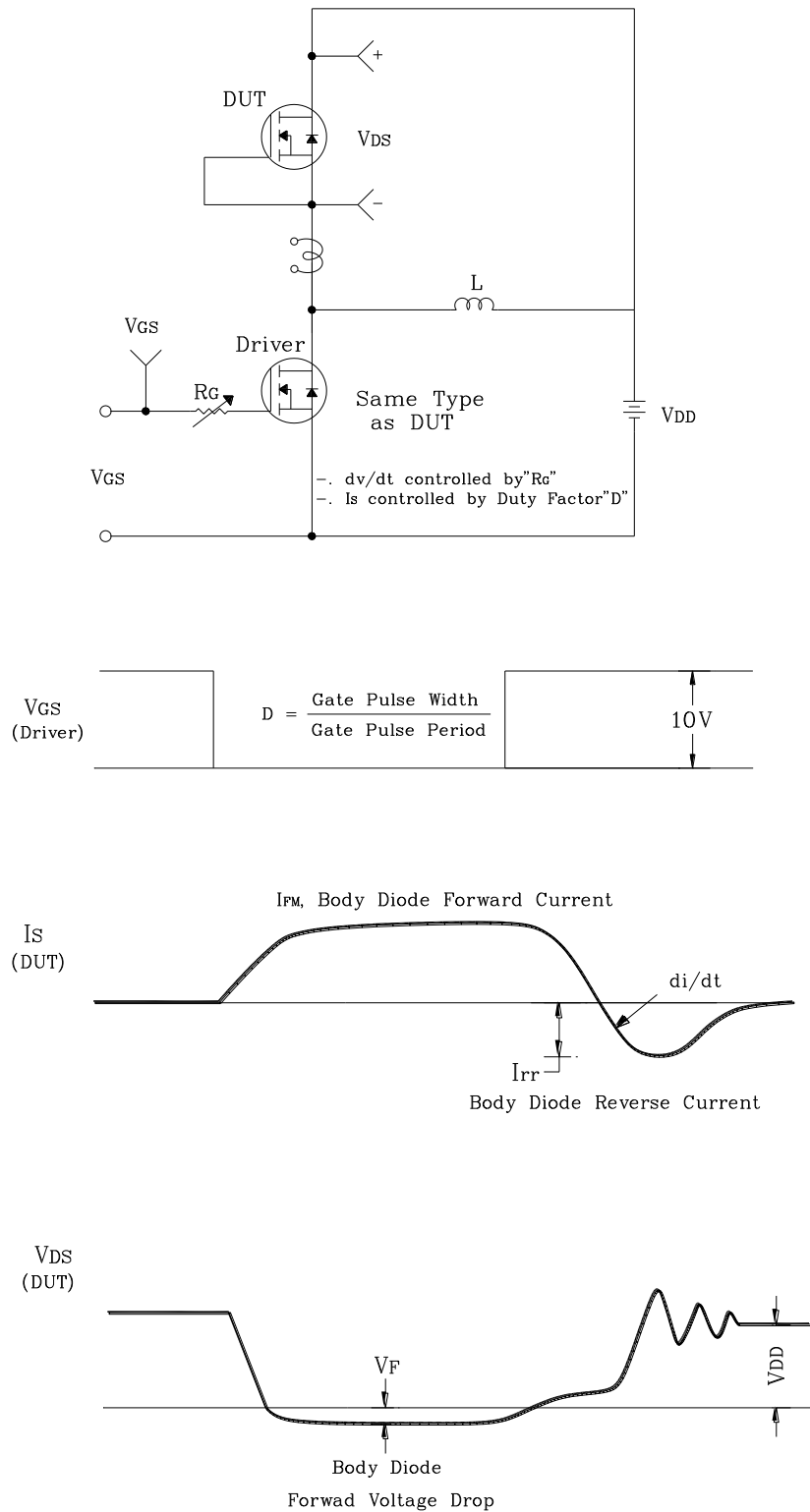
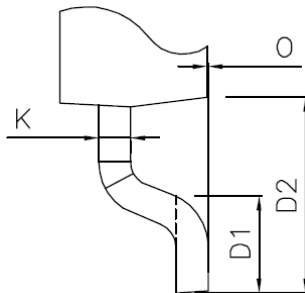
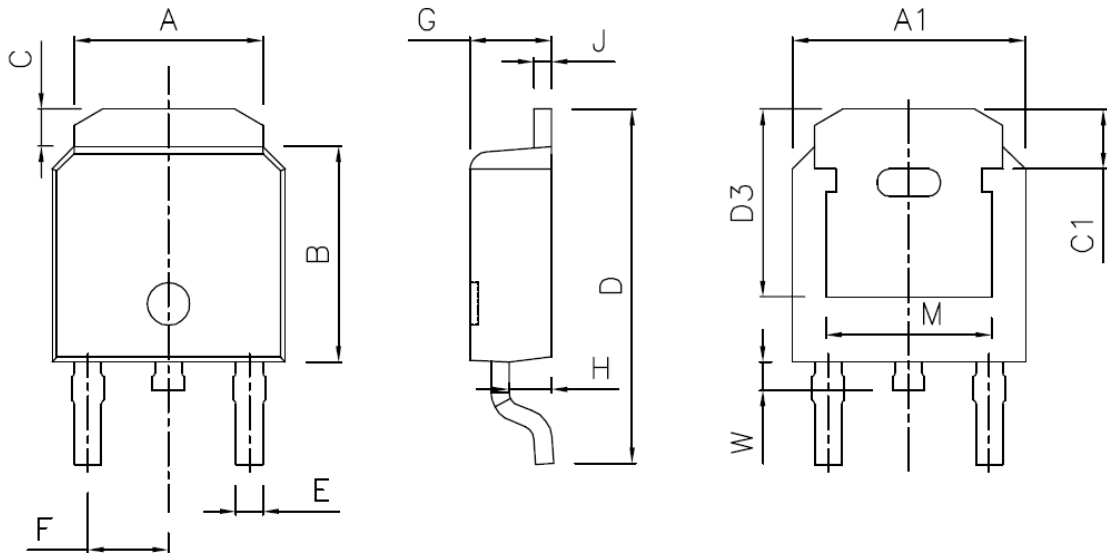


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS		
	MIN	NOR	MAX
A	5.03	5.34	5.64
A1	6.30	6.60	6.90
B	5.70	6.00	6.30
C	0.75	1.05	1.35
C1	1.021	1.321	1.621
D	9.65	9.95	10.25
D1	1.30	1.50	1.70
D2	2.70	2.90	3.10
D3	5.00	5.30	5.60
E	0.61	0.76	0.91
F	2.13	2.28	2.43
G	2.00	2.30	2.60
H	0.76	1.06	1.36
J	0.36	0.51	0.66
K	0.37	0.52	0.67
M	4.55	4.85	5.15
O	0.00	0.07	0.17
W	0.60	0.90	1.20

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