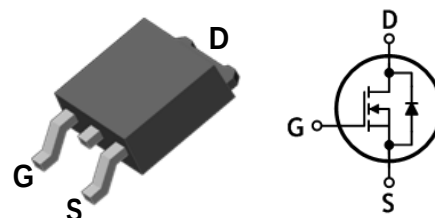


N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: $V_{DS}=650V$ (@ $T_J=150^{\circ}C$)
- Low drain-source On resistance: $R_{DS(on)}=0.6\Omega$ (Max.)
- Ultra low gate charge: $Q_g=13.5nC$ (Typ.)
- RoHS compliant device
- 100% avalanche tested

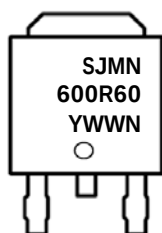


Ordering Information

Part Number	Marking	Package
SJMN600R60D	SJMN600R60	TO-252

TO-252

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWWN
 -. YWW: Date Code (year, week)
 -. N: Management Code

Absolute maximum ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	600	V
Gate-source voltage	V_{GSS}	± 30	V
Drain current (DC) (Note 1)	I_D	$T_C=25^{\circ}C$	7
		$T_C=100^{\circ}C$	4.4
Drain current (Pulsed) (Note 1)	I_{DM}	28	A
Single pulsed avalanche energy (Note 2)	E_{AS}	158	mJ
Repetitive avalanche current (Note 1)	I_{AR}	7	A
Repetitive avalanche energy (Note 1)	E_{AR}	6.3	mJ
Power dissipation	P_D	63	W
Diode dv/dt ruggedness (Note 3)	dv/dt	15	V/ns
MOSFET dv/dt ruggedness (Note 4)	dv/dt	50	V/ns
Junction temperature	T_J	150	$^{\circ}C$
Storage temperature range	T_{stg}	-55~150	$^{\circ}C$

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.98	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	2	3	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=600\text{V}$, $T_J=125^{\circ}\text{C}$	-	-	100	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3.5\text{A}$	-	0.5	0.6	Ω
Internal gate resistance	R_g	$f=1\text{MHz}$, Open drain	-	21	-	Ω
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	557	-	pF
Output capacitance	C_{oss}		-	294	-	
Reverse transfer capacitance	C_{rss}		-	17	-	
Turn-on delay time (Note 5)	$t_{d(on)}$	$V_{DS}=350\text{V}$, $I_D=7\text{A}$, $R_G=25\Omega$	-	16	-	ns
Rise time (Note 5)	t_r		-	13	-	
Turn-off delay time (Note 5)	$t_{d(off)}$		-	35	-	
Fall time (Note 5)	t_f		-	7	-	
Total gate charge (Note 6)	Q_g	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=7\text{A}$	-	13.5	-	nC
Gate-source charge (Note 6)	Q_{gs}		-	4.5	-	
Gate-drain charge (Note 6)	Q_{gd}		-	3.5	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	7	A
Source current (Pulsed)	I_{SM}		-	-	28	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=7\text{A}$	-	-	1.2	V
Reverse recovery time (Note 5, 6)	t_{rr}	$I_S=7\text{A}$, $V_{GS}=0\text{V}$, $dI_S/dt=100\text{A}/\mu\text{s}$	-	278	-	ns
Reverse recovery charge (Note 5, 6)	Q_{rr}		-	2	-	μC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. $L=7\text{mH}$, $I_{AS}=7\text{A}$, $V_{DP}=50\text{V}$, Starting $T_J=25^{\circ}\text{C}$
3. $I_S \leq 7\text{A}$, $V_{DS} \leq 400\text{V}$, $dI_S/dt \leq 100\text{A}/\mu\text{s}$, $T_J=25^{\circ}\text{C}$
4. $V_{DS} \leq 400\text{V}$, $I_S \leq 7\text{A}$
5. Guaranteed by design, not subject to production testing
6. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

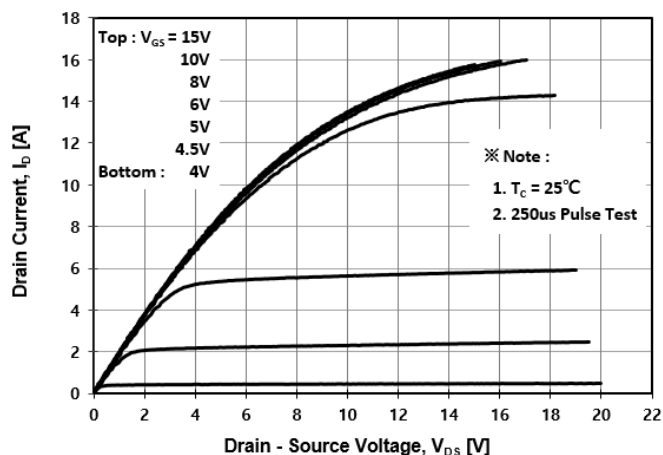


Fig. 2 Typical Transfer Characteristics

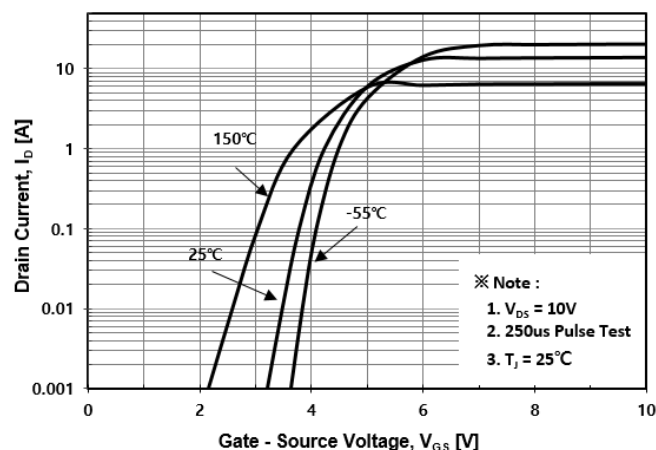


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

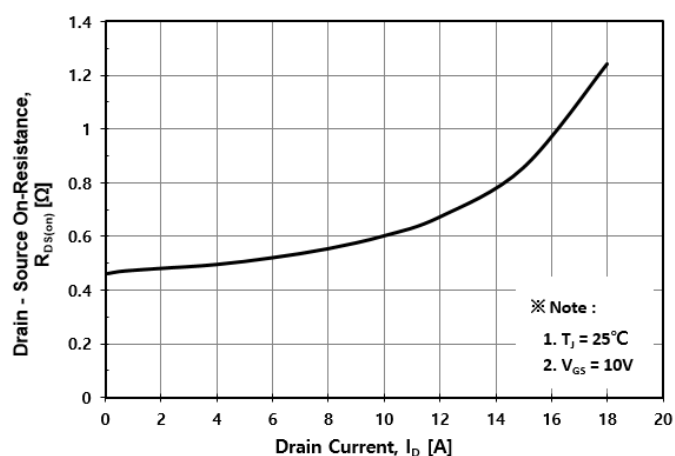


Fig. 4 Body Diode Forward Voltage Variation with Source Current

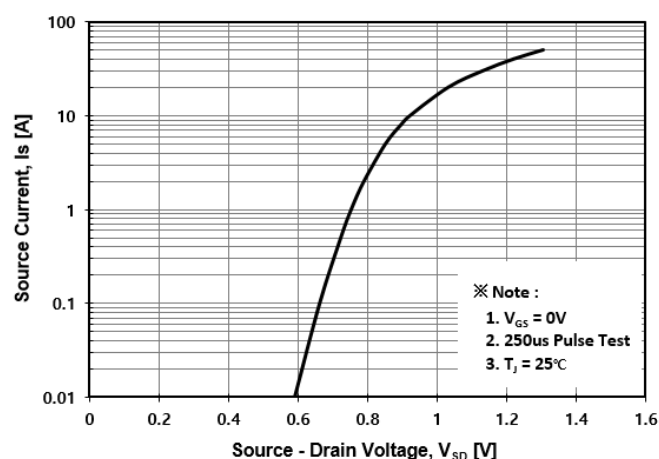


Fig. 5 Typical Capacitance Characteristics

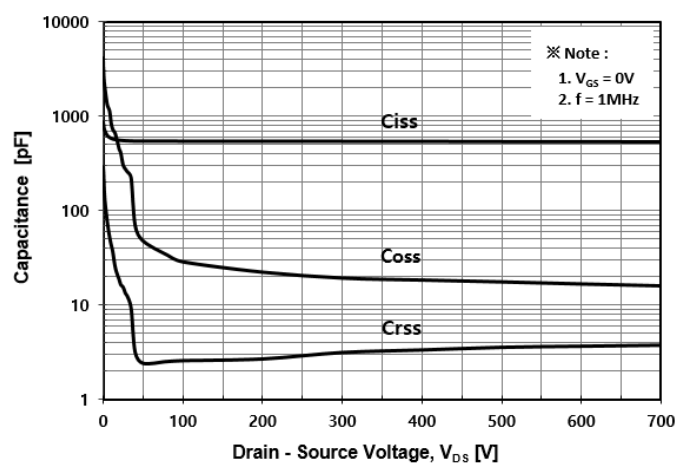


Fig. 6 Typical Total Gate Charge Characteristics

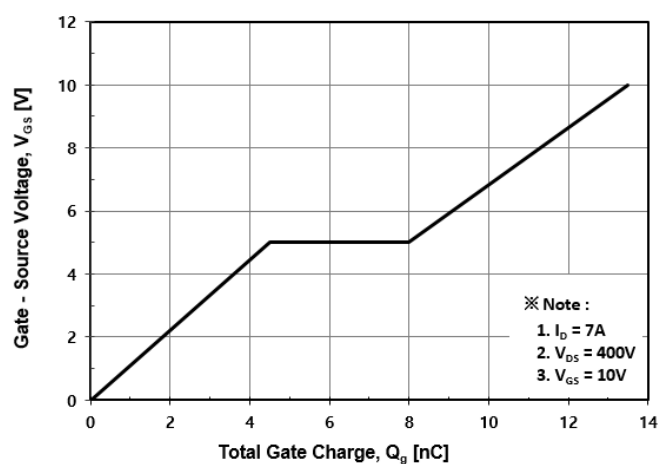


Fig. 7 Breakdown Voltage Variation vs. Temperature

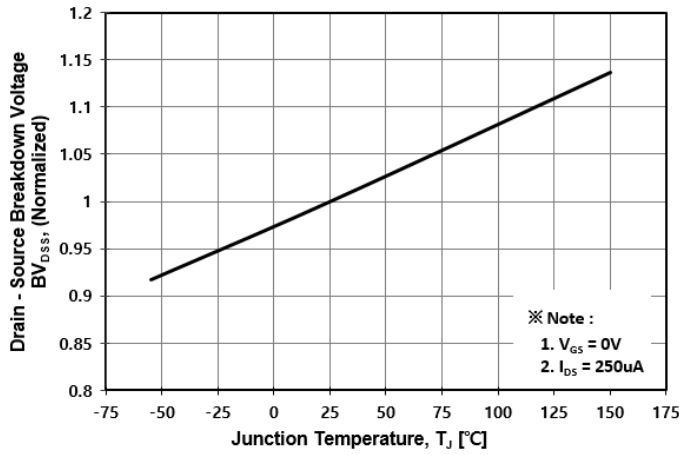


Fig. 8 On-Resistance Variation vs. Temperature

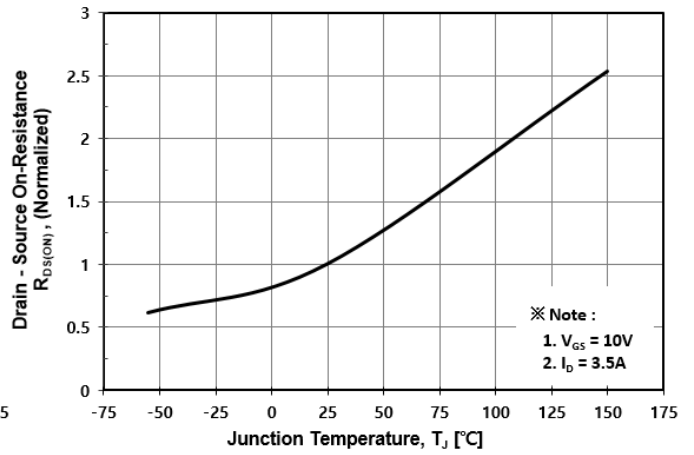


Fig. 9 Maximum Drain Current vs. Case Temperature

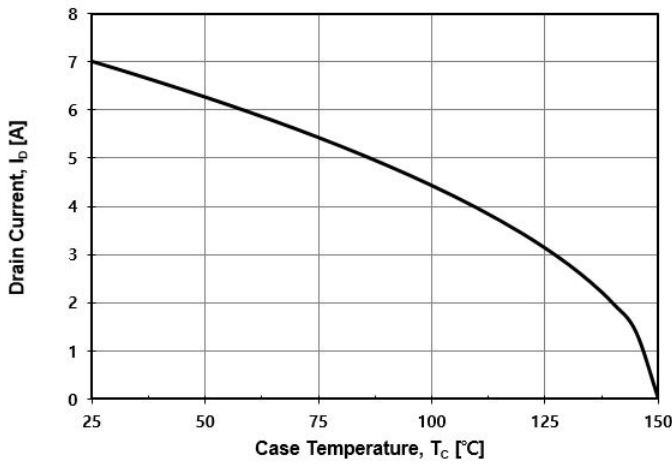


Fig. 10 Maximum Safe Operating Area

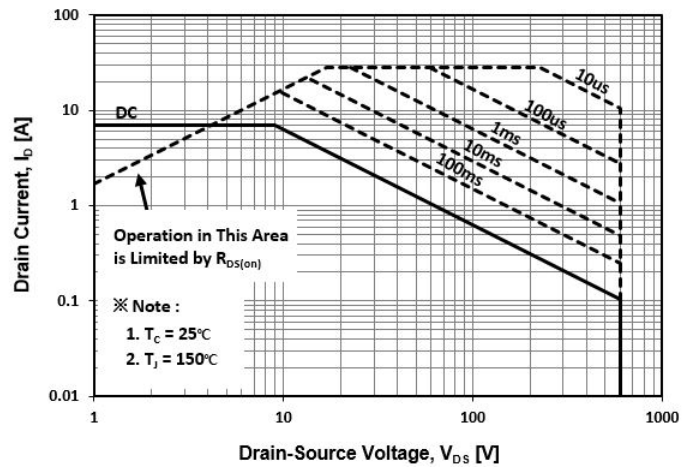


Fig. 11 Transient Thermal Impedance

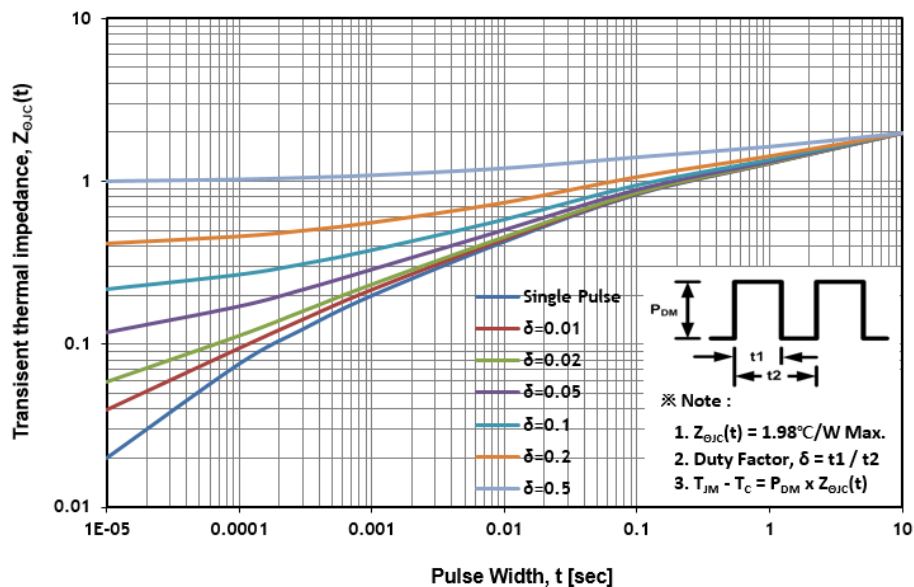


Fig. 12 Gate Charge Test Circuit & Waveform

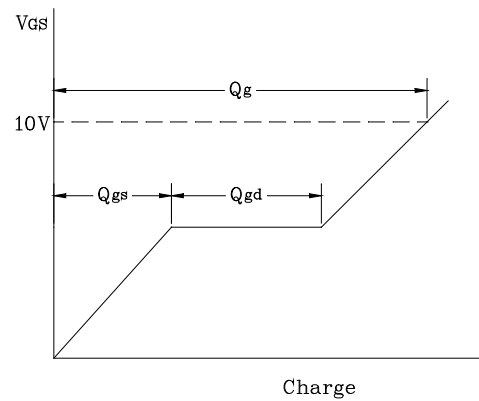
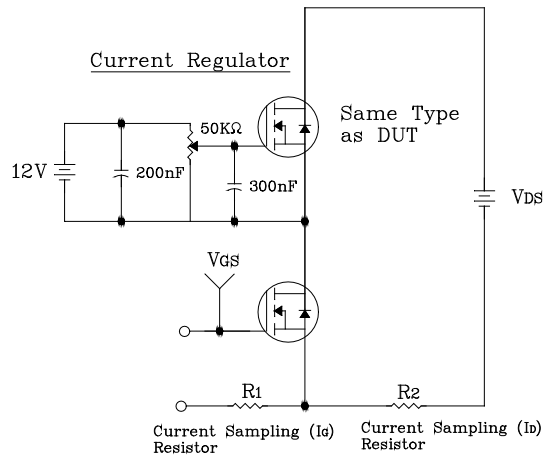


Fig. 13 Resistive Switching Test Circuit & Waveform

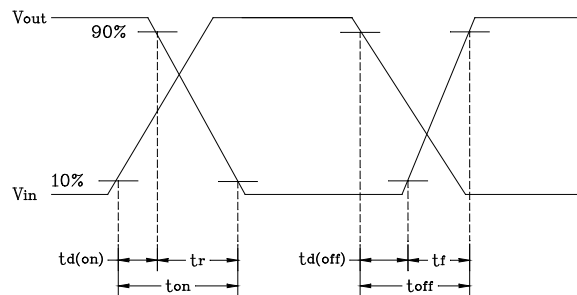
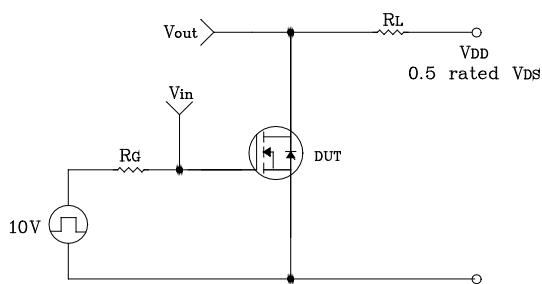
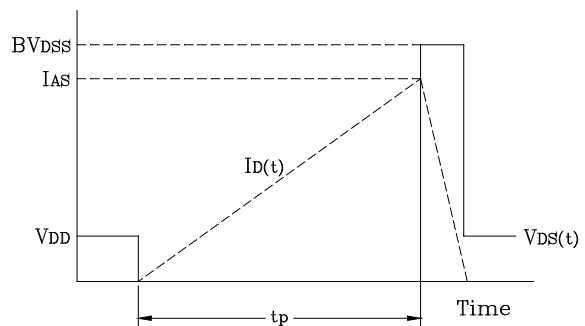
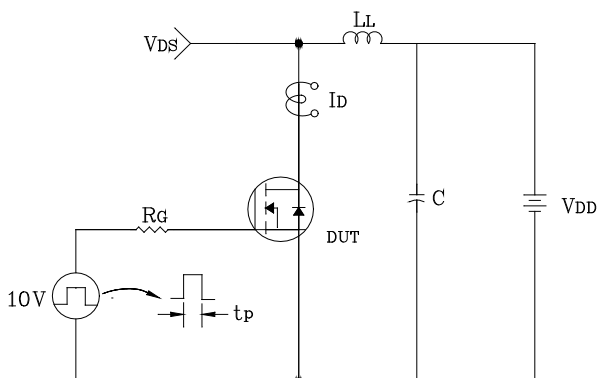
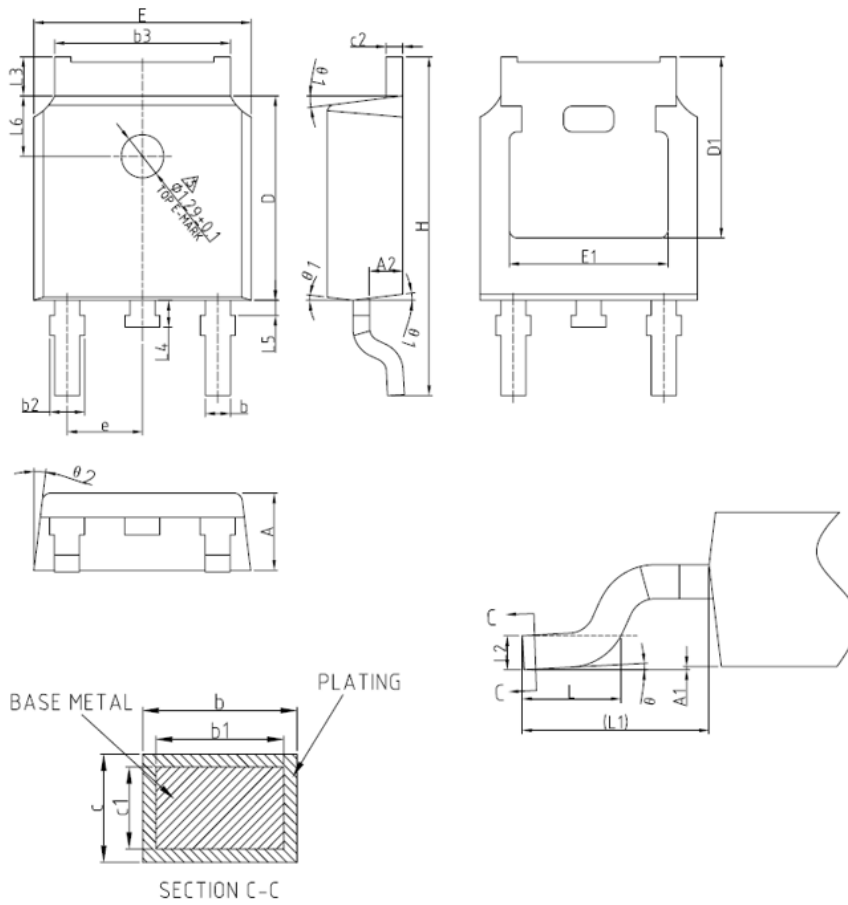


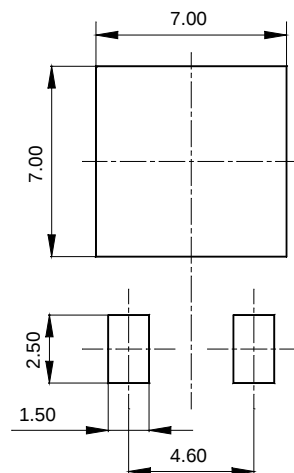
Fig. 14 E_{AS} Test Circuit & Waveform



Package Outline Dimensions



Recommended Land Pattern [unit: mm]



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