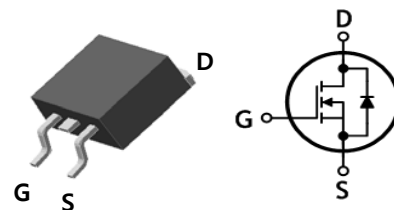


N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: $V_{DS}=700V$ (@ $T_J=150^{\circ}C$)
- Low drain-source On resistance: $R_{DS(on)}=0.18\Omega$ (Max.)
- Ultra low gate charge: $Q_g=32nC$ (Typ.)
- RoHS compliant and Halogen free device
- 100% avalanche tested

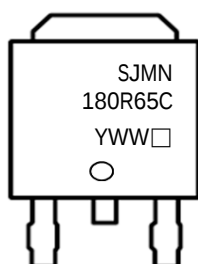


TO-263 (D²-PAK)

Ordering Information

Part Number	Marking	Package
SJMN180R65CB	SJMN180R65C	TO-263(D ² -PAK)

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g) YWW□
 -. YWW = Date Code (year, week)
 -. □ = Factory Management Code

Absolute maximum ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V _{DSS}		650	V
Gate-source voltage	V _{GSS}		±30	V
Drain current (DC) ^(Note 1)	I _D	T _c =25°C	22	A
		T _c =100°C	13.9	A
Drain current (Pulsed) ^(Note 1)	I _{DM}		88	A
Single pulsed avalanche energy ^(Note 2)	E _{AS}		160	mJ
Single avalanche current ^(Note 2)	I _{AS}		8	A
MOSFET dv/dt ruggedness (V _{DS} ≤400V)	dv/dt		50	V/ns
Diode dv/dt ruggedness (I _{SD} ≤I _D , V _{DS} ≤400V)	dv/dt		15	V/ns
Power dissipation	P _D		125	W
Junction temperature	T _J		150	°C
Storage temperature range	T _{stg}		-55~150	°C

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=1\text{mA}$, $V_{GS}=0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=1.2\text{mA}$, $V_{DS}=V_{GS}$	2.5	-	4.5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$	-	-	1	uA
		$V_{DS}=650\text{V}$, $T_J=125^\circ\text{C}$	-	-	100	uA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=8\text{A}$	-	0.15	0.18	Ω
Internal gate resistance	R_g	$f=1\text{MHz}$, Open drain	-	1.5	-	Ω
Input capacitance (Note 3, 4)	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	1302	-	pF
Output capacitance (Note 3, 4)	C_{oss}		-	1203	-	
Reverse transfer capacitance (Note 3, 4)	C_{rss}		-	50	-	
Turn-on delay time (Note 3, 4)	$t_{d(on)}$	$V_{DS}=350\text{V}$, $I_D=22\text{A}$, $R_G=25\Omega$	-	35	-	ns
Rise time (Note 3, 4)	t_r		-	35	-	
Turn-off delay time (Note 3, 4)	$t_{d(off)}$		-	77	-	
Fall time (Note 3, 4)	t_f		-	38	-	
Total gate charge (Note 3, 4)	Q_g	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=10\text{A}$	-	32	-	nC
Gate-source charge (Note 3, 4)	Q_{gs}		-	10	-	
Gate-drain charge (Note 3, 4)	Q_{gd}		-	12	-	

Source-Drain Diode Ratings and Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	22	A
Source current (Pulsed)	I_{SM}		-	-	88	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=8\text{A}$	-	-	1.2	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=22\text{A}$, $V_{GS}=0\text{V}$, $dI_S/dt=100\text{A/us}$	-	418	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	7.9	-	uC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. $L=5\text{mH}$, $V_{DD}=50\text{V}$, Starting $T_J=25^\circ\text{C}$
3. Guaranteed by design, not subject to production testing
4. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

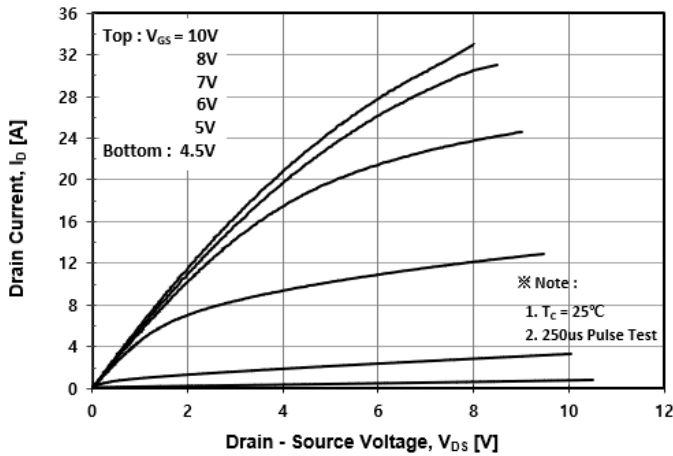


Fig. 2 Typical Transfer Characteristics

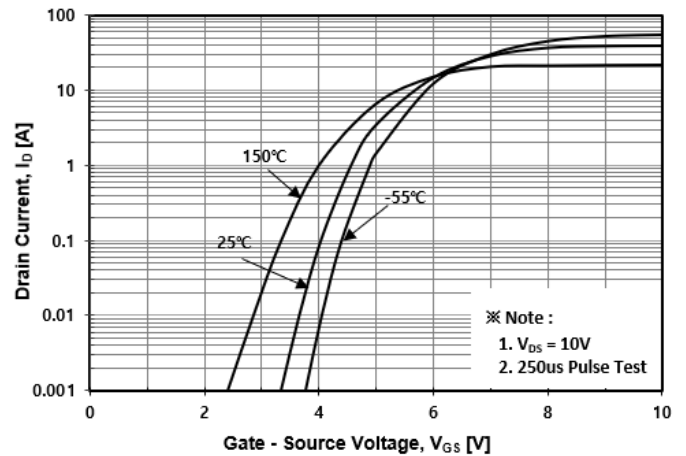


Fig. 3 On-Resistance Variation with Drain Current and Gate Voltage

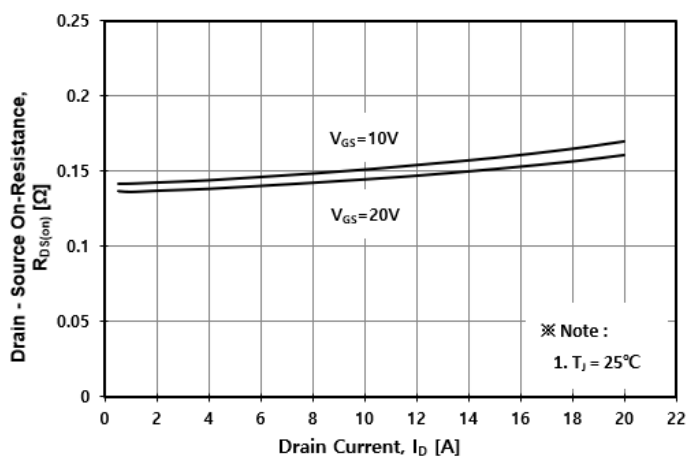


Fig. 4 Body Diode Forward Voltage Variation with Source Current

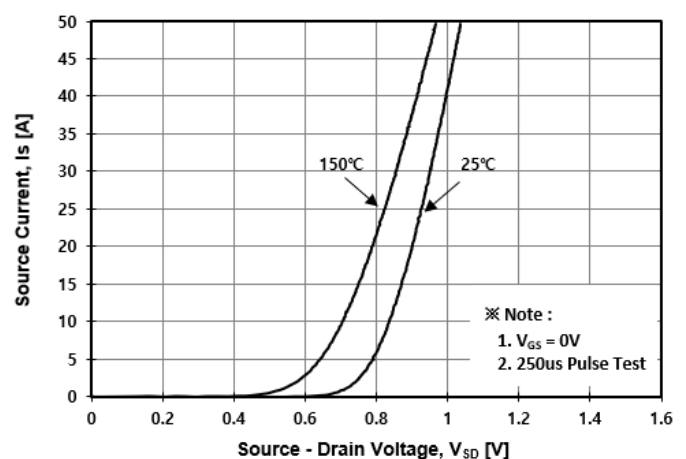


Fig. 5 Typical Capacitance Characteristics

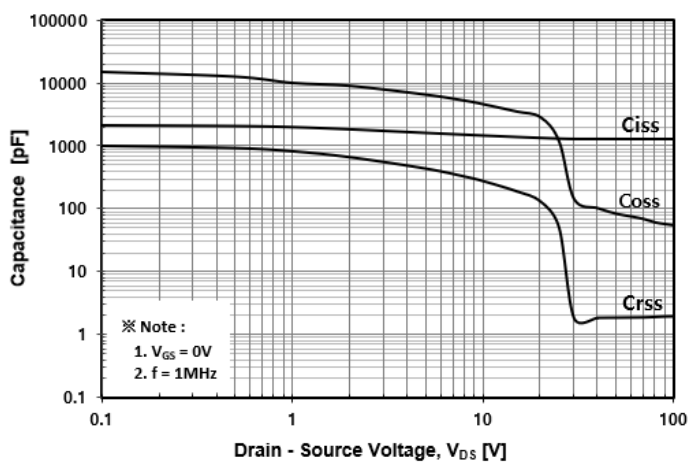
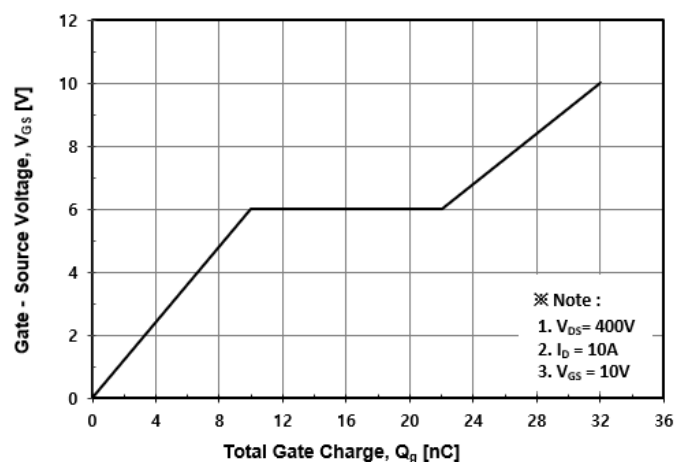


Fig. 6 Typical Total Gate Charge Characteristics



Typical Electrical Characteristics Curves

Fig. 7 Breakdown Voltage Variation vs. Temperature

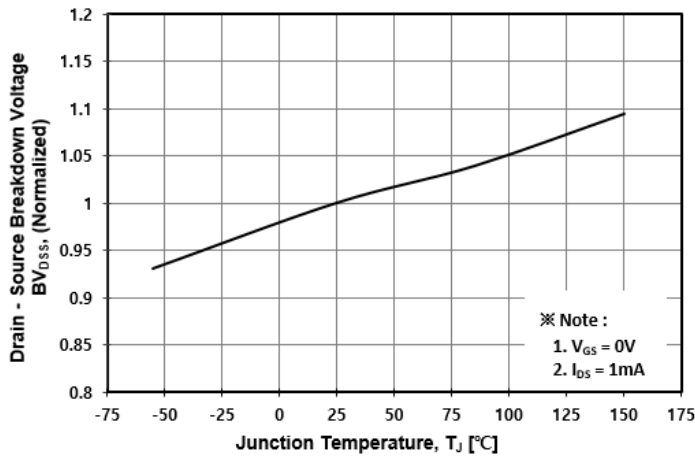


Fig. 8 On-Resistance Variation vs. Temperature

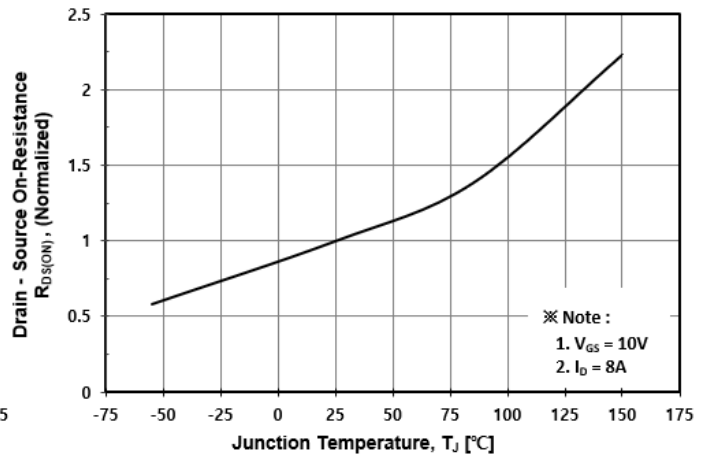


Fig. 9 Maximum Drain Current vs. Case Temperature

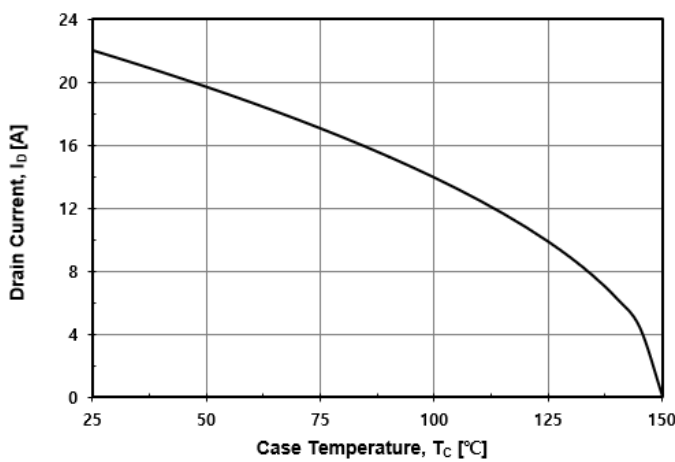


Fig. 10 Maximum Safe Operating Area

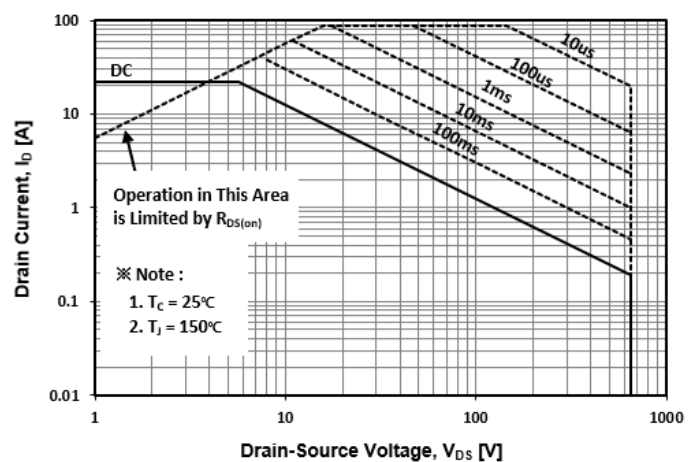


Fig. 11 Transient Thermal Impedance

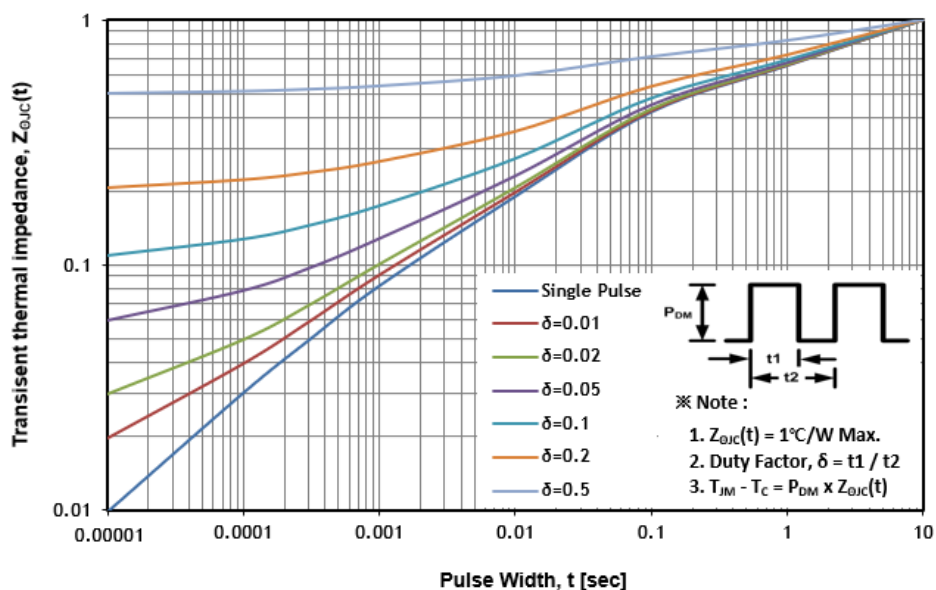


Fig. 12 Gate Charge Test Circuit & Waveform

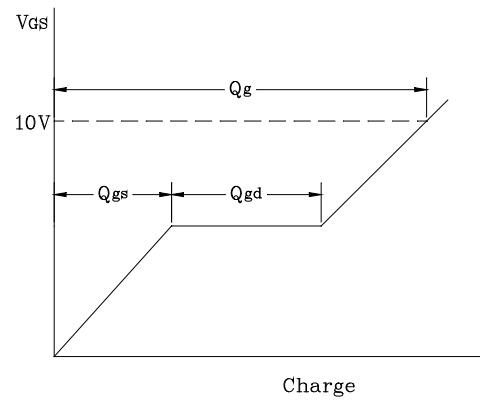
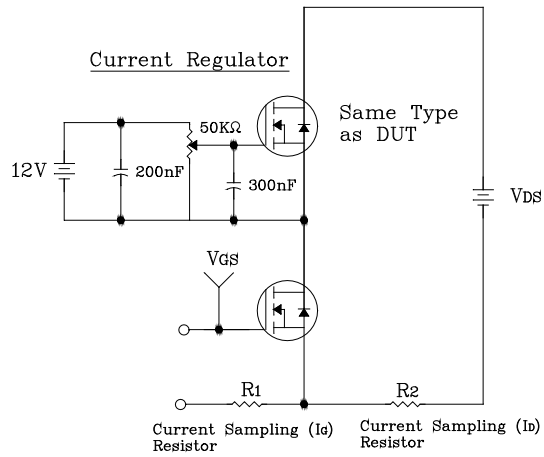


Fig. 13 Resistive Switching Test Circuit & Waveform

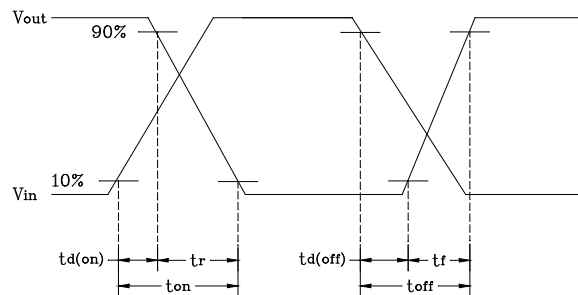
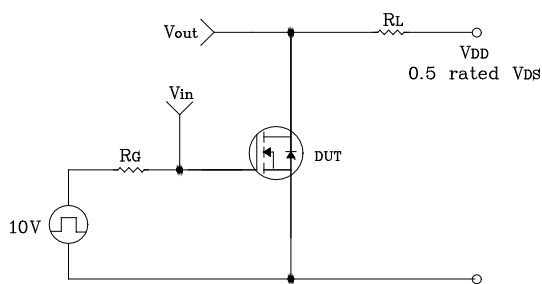


Fig. 14 EAS Test Circuit & Waveform

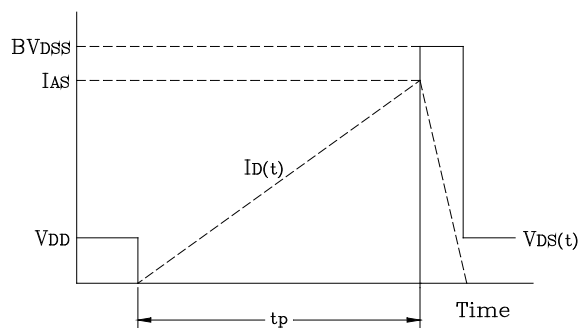
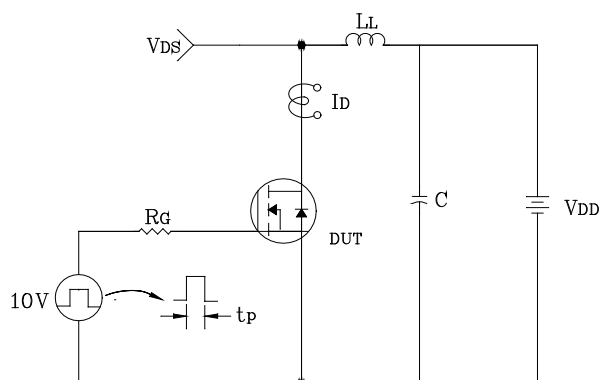
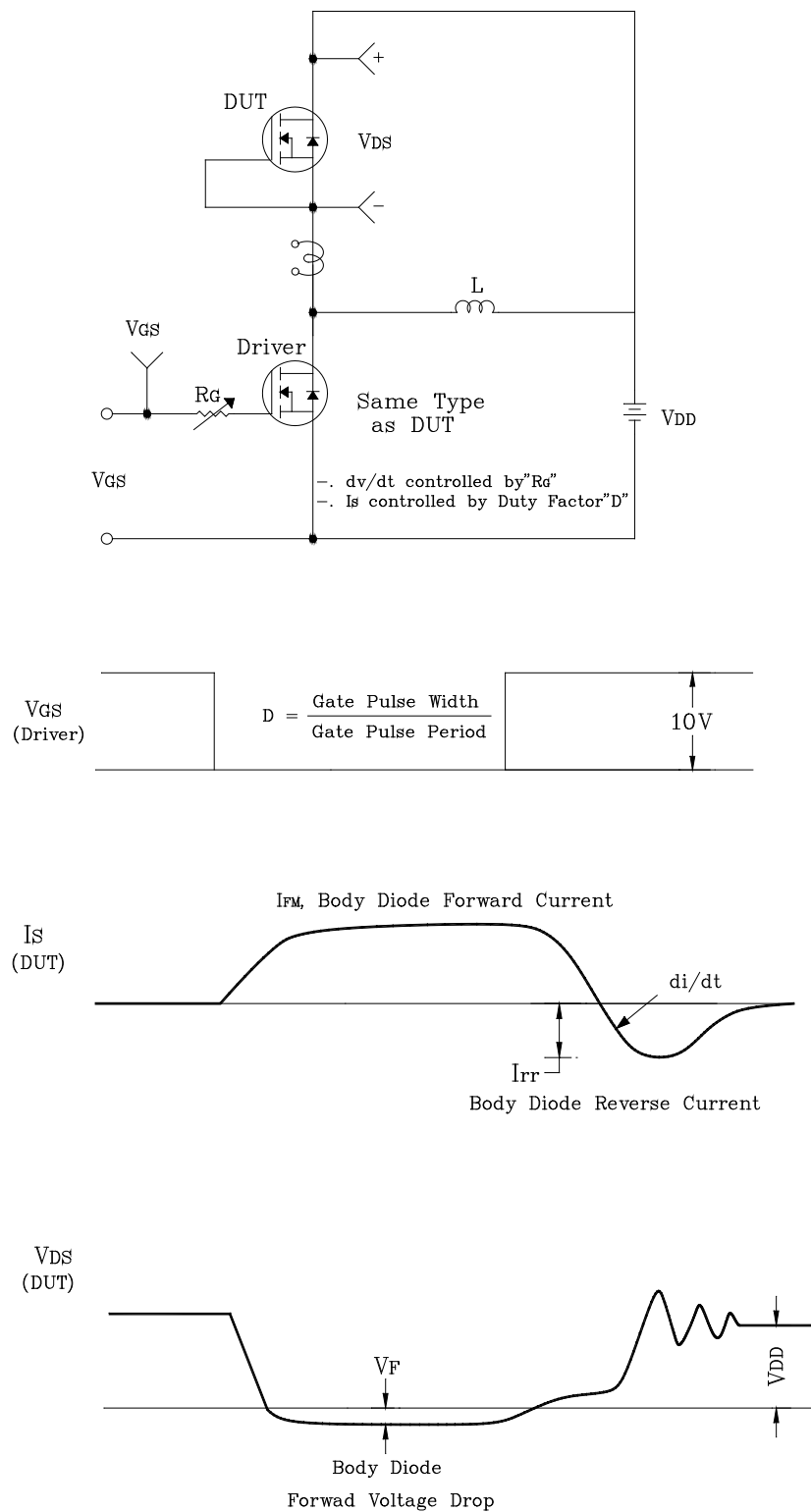
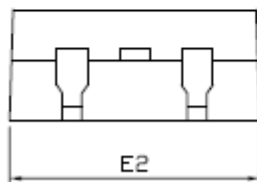
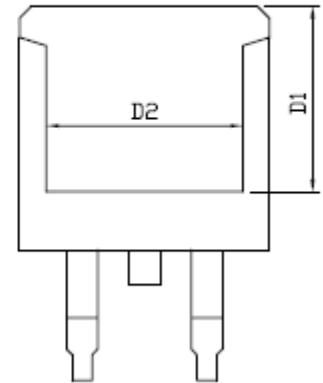
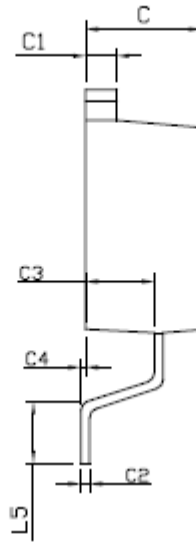
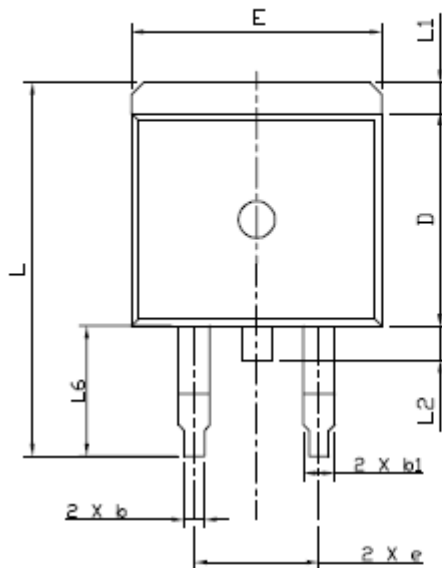


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
b	0.73	0.80	0.87
b1	1.20	1.27	1.34
C	4.38	4.48	4.58
C1	1.23	1.30	1.37
C2	0.43	0.50	0.57
C3	2.25	2.40	2.55
C4	0.02	0.10	0.18
D	9.10	9.20	9.30
D2	7.90	8.00	8.10
E	9.78	9.88	9.98
e	4.98	5.08	5.18
E2	9.75	9.90	10.05
L	14.95	15.20	15.45
L1	1.15	1.30	1.45
L2	1.50	1.60	1.70
L5	2.25	2.40	2.55
L6	4.60	4.80	5.00

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