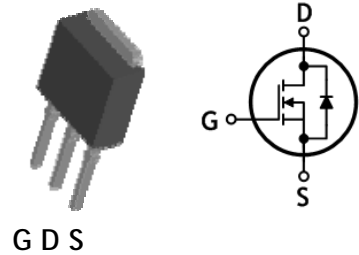


SWITCHING REGULATOR APPLICATION

Features

- $BV_{DSS}=880V @T_{jmax}$
- Low gate charge: $Q_g=19nC$ (Typ.)
- Low drain-source On resistance: $R_{DS(on)}=4.2\Omega$ (Max.)
- RoHS compliant device
- Halogen free package



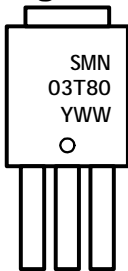
G D S

I-PAK

Ordering Information

Part Number	Marking	Package
SMN03T80IS	SMN03T80	I-PAK (Short Lead)

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW
 - . YWW: Date Code (year, week)

Absolute maximum ratings ($T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V_{DSS}	800	V	
Gate-source voltage	V_{GSS}	± 30	V	
Drain current (DC) *	I_D	$T_c=25^\circ C$	3	A
		$T_c=100^\circ C$	1.83	A
Drain current (Pulsed) *	I_{DM}	12	A	
Single pulsed avalanche energy ^(Note 2)	E_{AS}	200	mJ	
Repetitive avalanche current ^(Note 1)	I_{AR}	3	A	
Repetitive avalanche energy ^(Note 1)	E_{AR}	7	mJ	
Power dissipation	P_D	70	W	
Peak diode recovery dv/dt ^(Note 3)	dv/dt	4.5	V/ns	
Junction temperature	T_J	150	$^\circ C$	
Storage temperature range	T_{stg}	-55~150	$^\circ C$	

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.78	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 110	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}, V_{GS}=0$	800	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$	2	-	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=800\text{V}, V_{GS}=0\text{V}$	-	-	10	μA
		$V_{DS}=640\text{V}, T_C=125^\circ\text{C}$	-	-	100	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=1.5\text{A}$	-	3.36	4.2	Ω
Forward transfer conductance (Note 4)	g_{fs}	$V_{DS}=30\text{V}, I_D=1.5\text{A}$	-	3.7	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$	-	696	-	pF
Output capacitance	C_{oss}		-	65	-	
Reverse transfer capacitance	C_{rss}		-	10.2	-	
Turn-on delay time (Note 4,5)	$t_{d(on)}$	$V_{DD}=400\text{V}, I_D=3\text{A}, R_G=25\Omega$	-	48	-	ns
Rise time (Note 4,5)	t_r		-	36	-	
Turn-off delay time (Note 4,5)	$t_{d(off)}$		-	106	-	
Fall time (Note 4,5)	t_f		-	41	-	
Total gate charge (Note 4,5)	Q_g	$V_{DS}=640\text{V}, V_{GS}=10\text{V}, I_D=3\text{A}$	-	19	-	nC
Gate-source charge (Note 4,5)	Q_{gs}		-	4	-	
Gate-drain charge (Note 4,5)	Q_{gd}		-	7.6	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	3	A
Source current (Pulsed)	I_{SM}		-	-	12	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}, I_S=3\text{A}$	-	-	1.5	V
Reverse recovery time (Note 4,5)	t_{rr}	$I_S=3\text{A}, V_{GS}=0\text{V}, di/dt=100\text{A}/\mu\text{s}$	-	372	-	ns
Reverse recovery charge (Note 4,5)	Q_{rr}		-	1.8	-	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=42\text{mH}, I_{AS}=3\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. $I_{SD}\leq 3\text{A}, di/dt\leq 200\text{A}/\mu\text{s}, V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
4. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature typical characteristics

Electrical Characteristic Curves

Fig. 1 $I_D - V_{DS}$

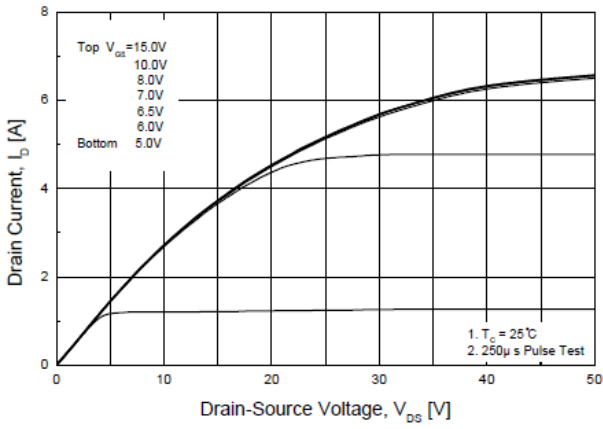


Fig. 2 $I_D - V_{GS}$

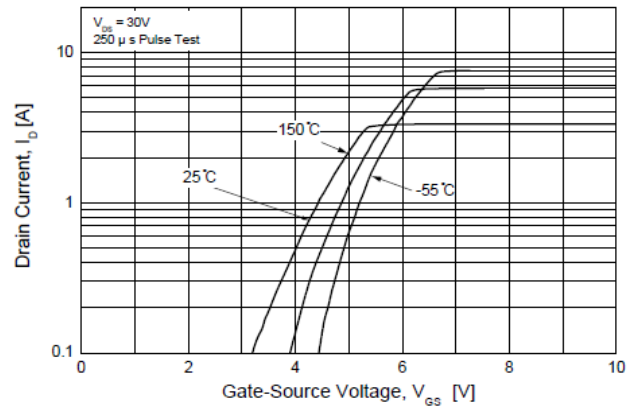


Fig. 3 $R_{DS(ON)} - I_D$

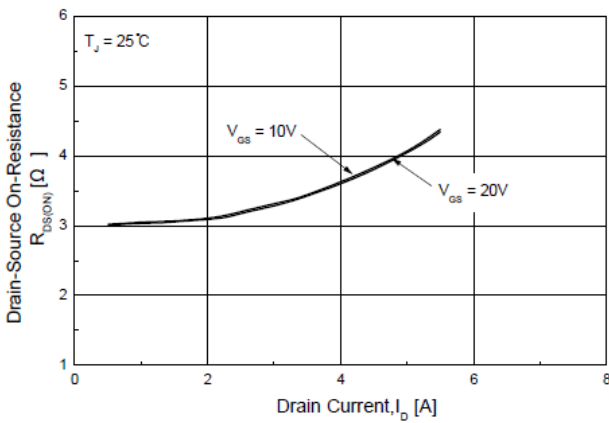


Fig. 4 $I_{DR} - V_{SD}$

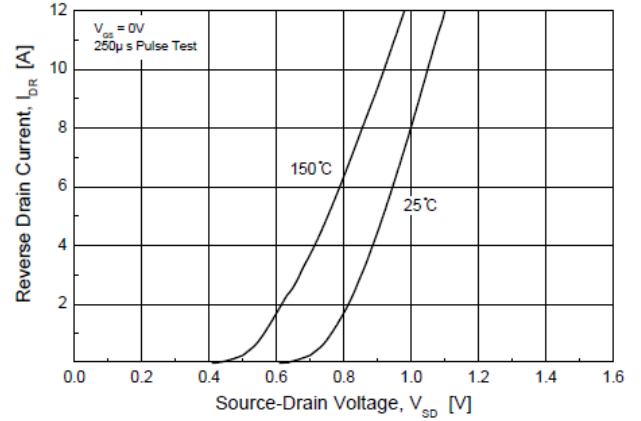


Fig. 5 Capacitance - V_{DS}

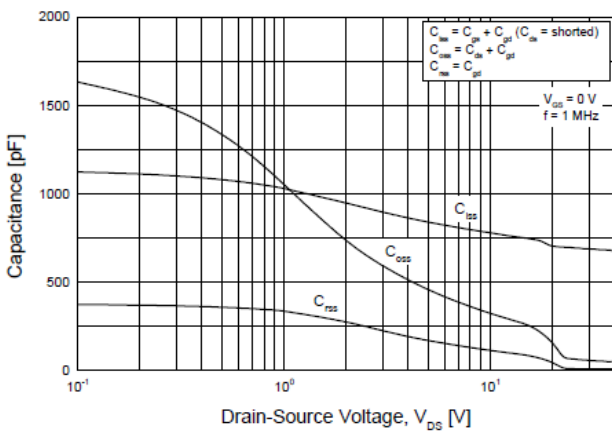
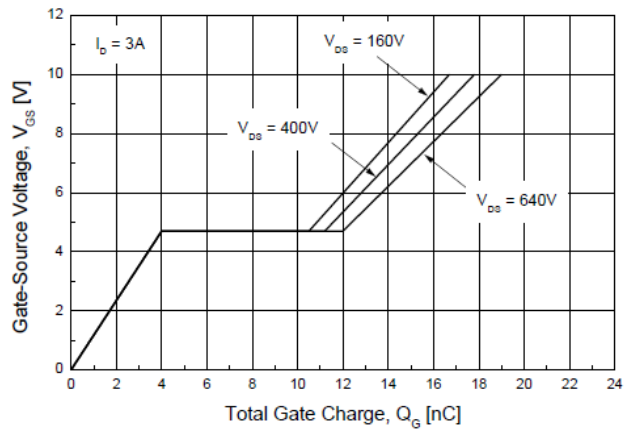


Fig. 6 $V_{GS} - Q_G$



Electrical Characteristic Curves (Continue)

Fig. 7 $BV_{DSS} - T_J$

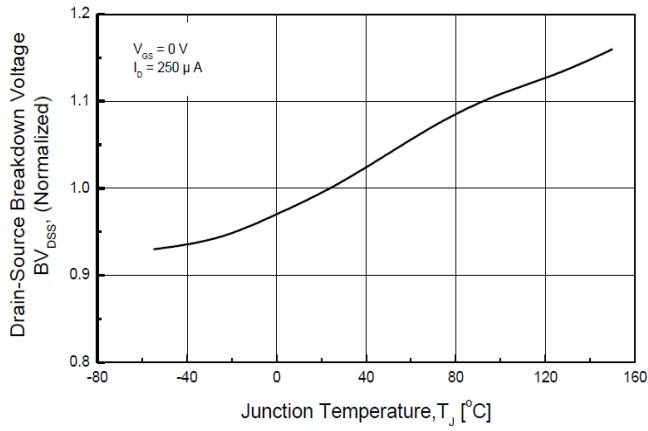


Fig. 8 $R_{DS(ON)} - T_J$

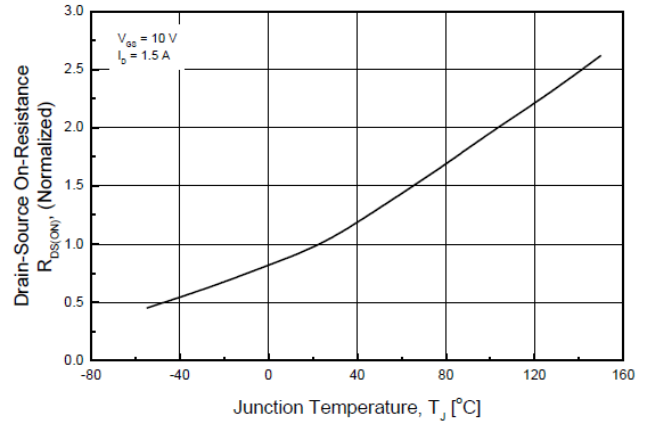


Fig. 9 $I_D - T_C$

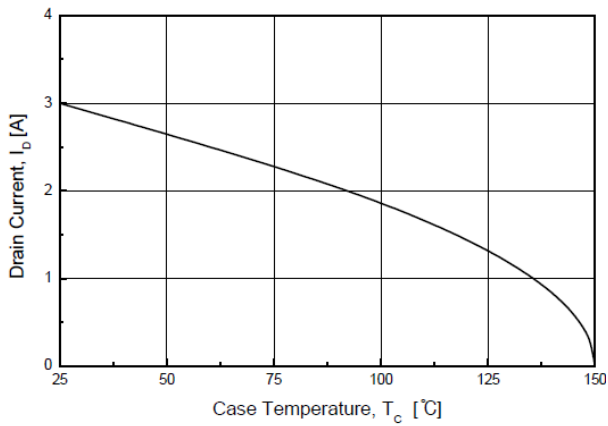


Fig. 10 $V_{GS(th)} - T_J$

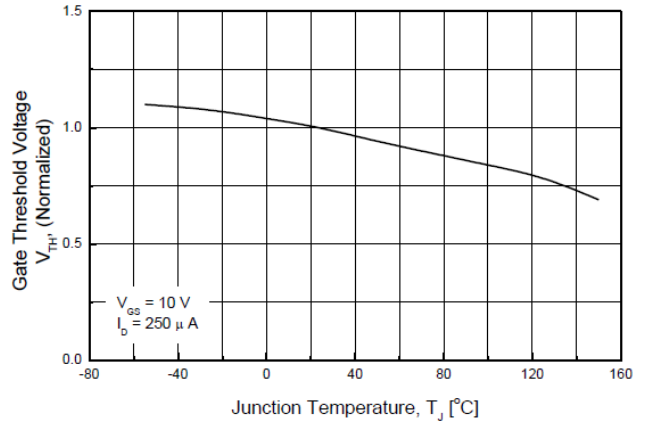


Fig. 11 Safe Operating Area

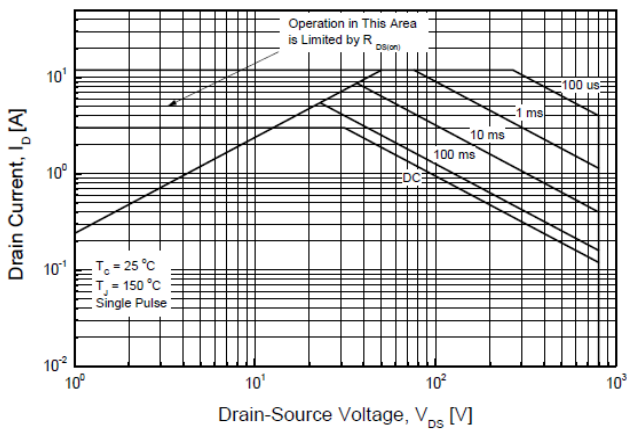


Fig. 12 $Z_{th(j-c)} - t$

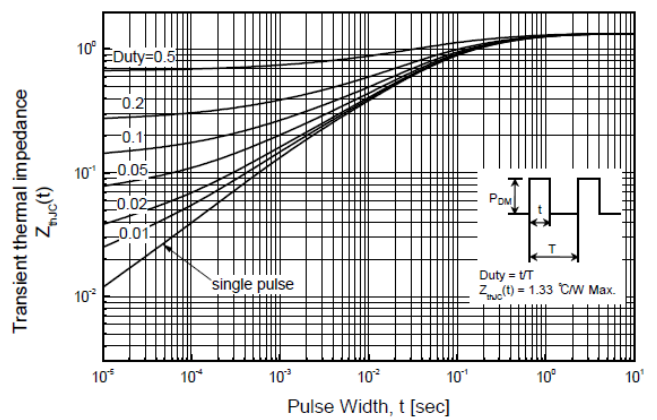


Fig. 13 Gate Charge Test Circuit & Waveform

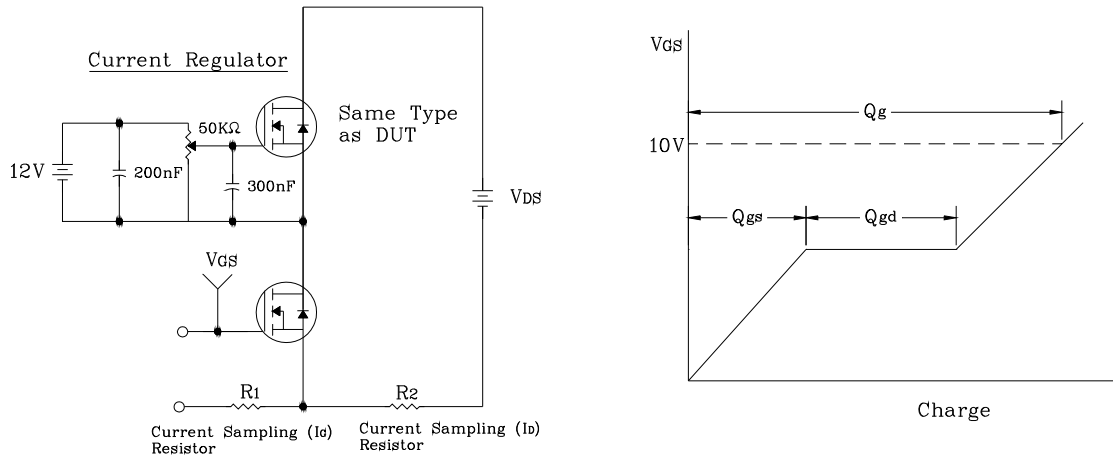


Fig. 14 Resistive Switching Test Circuit & Waveform

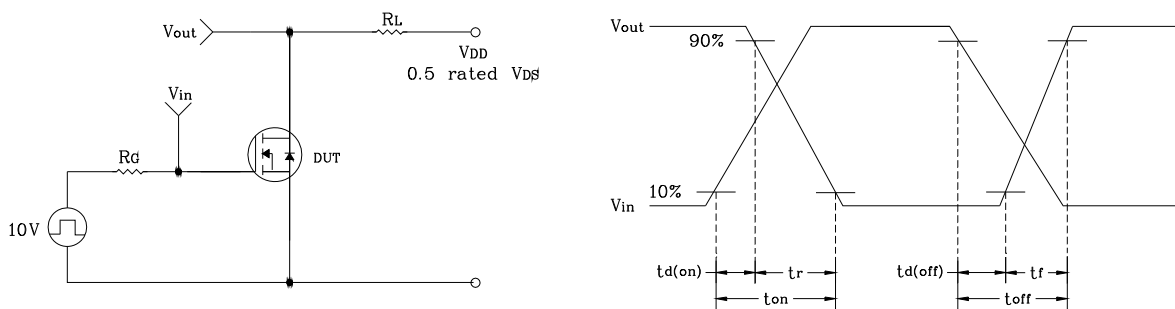


Fig. 15 E_{AS} Test Circuit & Waveform

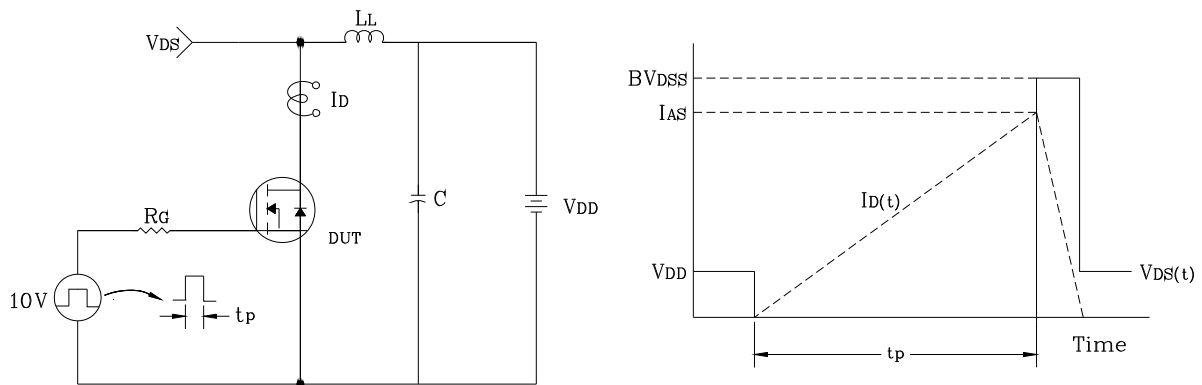
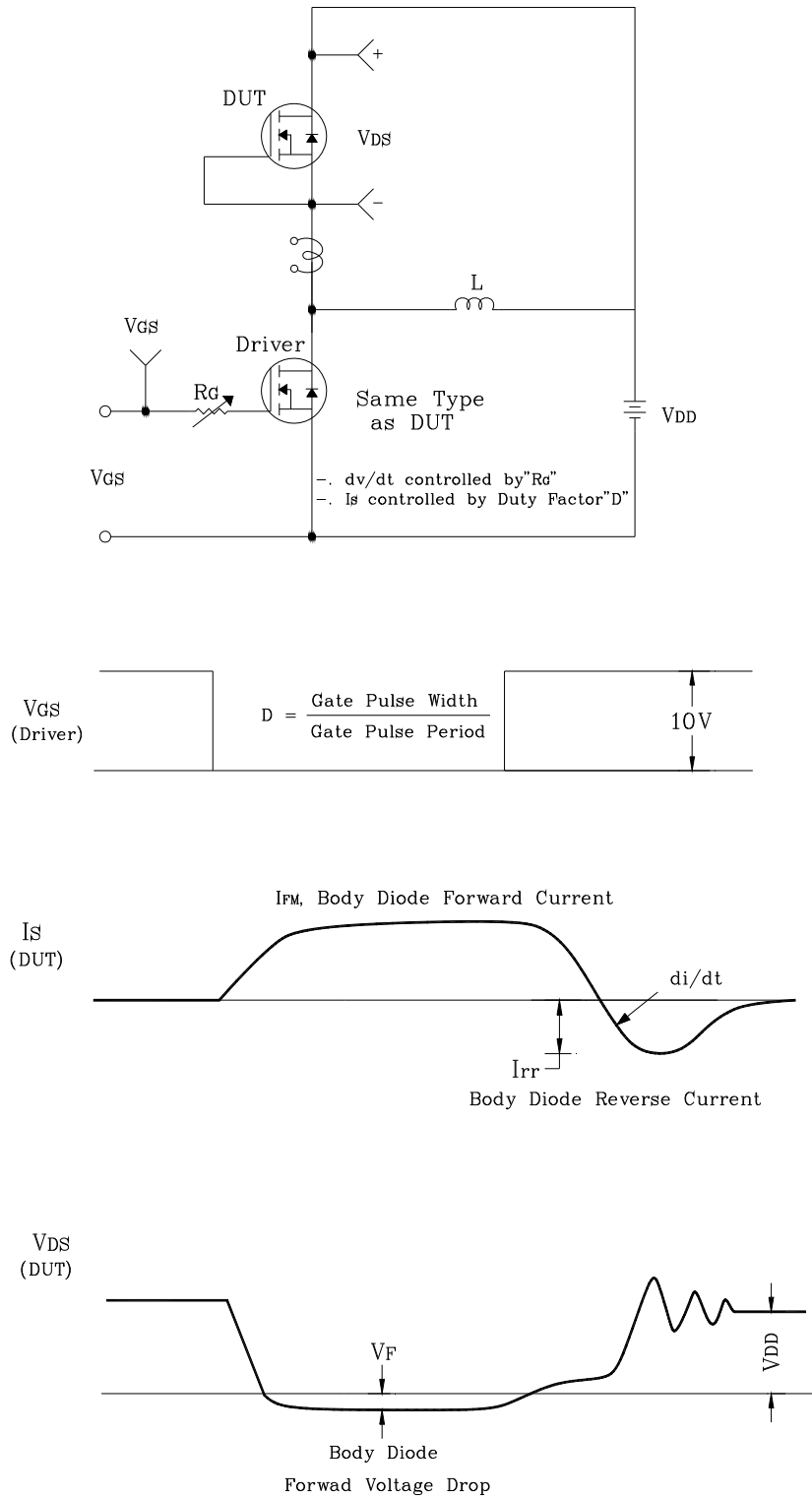


Fig. 16 Diode Reverse Recovery Time Test Circuit & Waveform



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